1.88 nA Quiescent Current Capacitor-Less LDO with Adaptive Biasing Based on a SSF Absolute Voltage Difference Meter

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***Abstract*—An ultra-low power LDO regulator with an adaptive biasing error amplifier is presented in this paper. An absolute difference voltage meter circuit section based on super source followers is used to achieve the adaptive biasing scheme. The experimental total quiescent current consumption is as low as 1.88 nA with a measured line sensitivity of 0.13 mV/V in a circuit occupying 1473 μm^2 of silicon area.**

I. Introduction

The most important restriction in battery operated systems such as internet of things (IoT) nodes and wearable or biomedical devices is power consumption. This aspect becomes of paramount importance when the powering system is based on energy harvesting. Indeed, the scavenged power is in general so reduced that the use of ultra-low-power consumption circuits becomes essential.

Photovoltaic harvesters for implantable micro-power applications, such as an intraocular biomedical device, have been implemented by integrating the solar cell, i.e, a photodiode, and the power management unit (PMU) in the same silicon substrate [1]. As a result, a small form factor may be additionally obtained. Furthermore, it is worth to point out that voltage regulation is required at the output of the PMU, so that a constant and continuous supply may be granted to the load regardless of the current level demanded.

The conventional implementation of a low drop-out (LDO) regulator [2] consists of an error amplifier (EA), a pass transistor, M_{pass} and a passive feedback network. The feedback action implicit in the LDO allows setting the output voltage as a function of a reference voltage, V_{ref}, by properly sizing devices in the feedback loop and settling the feedback factor. Besides, the maximum current that may be delivered to the load depends on the size and source-gate voltage of M_{pass}. In the context of energy harvesting powering, a very reduced quiescent bias current is required to allow ultra-low-power consumption. Nevertheless, the maximum current delivered to the load could be some orders of magnitude higher, thus requiring a large aspect ratio for M_{pass}. Besides, it is not only important the value of the maximum allowable output current, but also featuring a rapid load transient. As a consequence, the drive capability of the EA becomes a key point in the design of the LDO, so that it is able to properly drive the pass transistor in extreme loading conditions with a reduced power consumption in the standby operation.

The super-source-follower (SSF) [3] is an improved voltage follower able to deliver a maximum output current much higher than its quiescent bias current. This basic building block has been previously reported in the implementation of an LDO, particularly at the output stage to increase the driving capability of the pass transistor [4], [5]. Alternatively, it may be used to design an adaptive biasing scheme for the EA, ensuring reduced quiescent power consumption and granting high drive capability in the dynamic operation. This contribution introduces an LDO with an adaptive biasing section based on the SSF. The voltage regulator is able to deliver an output current in the order of mA with a quiescent bias current as low as 1.88 nA.

II. SSF voltage difference meter

The schematic of a super source follower (SSF) with NMOS input transistor is shown in Fig. 1a. The output voltage of this block, V_o, depends on the aspect ratio of transistor M_1 and its biasing current, I_{bias1}, factors that determine the gate-to-source voltage V_i–V_o of this device. Thus, the output voltage is given by (1), where ΔV is the gate-to-source voltage of M_1, shown in (2) for weak inversion (W.I.) and strong inversion (S.I.), I_{sn} is the characteristic current of the NMOS transistor, μ_n the electron mobility, C_{ox} the gate capacitance, n the subthreshold slope factor, V_T the thermal potential and V_{th} the threshold voltage.

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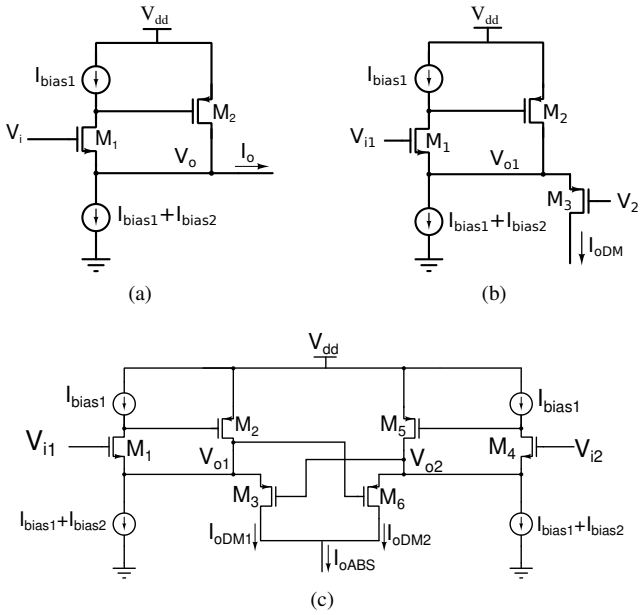


Fig. 1: (a) NMOS input SSF. (b) SSF-based voltage difference meter. (c) SSF AVDM circuit.

$$V_o = V_i - \Delta V \tag{1}$$

$$\Delta V = \begin{cases} V_{th1} + nV_T[ln\frac{I_{bias1}}{I_{sn}} - ln\frac{W_1}{L_1}] & \text{W.I.} \\ V_{th1} + \sqrt{\frac{2I_{bias1}}{\mu_n C_{ox}}\frac{L_1}{W1}} & \text{S.I.} \end{cases} \tag{2}$$

The maximum output current of the SSF, $I_{o,max}$, will be determined by the minimum voltage at the drain of M_1 that ensures its saturation, $V_{dM1,min}$, the aspect ratio of M_2, W_2/L_2, and the biasing current I_{bias2}. Assuming that M_2 will be in strong inversion at the maximum output current in the SSF, $I_{o,max}$ takes the form of (3), where μ_p is the hole mobility and $V_{dM1,min}$ is given by (4).

$$I_{o,max} = \frac{1}{2}\mu_p C_{ox}\frac{W_2}{L_2}(V_{dd} - V_{dM_1,min} + V_{th2}) - I_{bias2} \tag{3}$$

$$V_{dM_1,min} = \begin{cases} V_i - \Delta V_{(W.I.)} + 4V_T & M_1 \text{ in W.I.} \\ V_i - V_{th1} & M_1 \text{ in S.I.} \end{cases} \tag{4}$$

Adding a PMOS transistor M_3 as in Fig. 1b, the SSF can be used to compare two voltages, in this case V_{o1} and V_2, obtaining an output current I_{oDM} that depends on the voltage difference $V_{o1} - V_2$, as shown in (5).

$$I_{oDM} = \begin{cases} I_{sp}\frac{W_3}{L_3}e^{\frac{V_{o1}-V_2+V_{th3}}{nV_T}} & M_3 \text{ in W.I.} \\ \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(V_{o1} - V_2 + V_{th3})^2 & M_3 \text{ in S.I.} \end{cases} \tag{5}$$

To generate an output current that depends on the absolute difference between two voltages, two mirrored SSF as voltage difference meters must be used. In so doing, two shifted values of the input voltages, V_{o1} and V_{o2}, are compared, and so are indirectly V_{i1} and V_{i2}. The schematic of such a SSF absolute voltage difference meter (AVDM) circuit is shown in Fig. 1c.

Applying (1), (2) and (5) to the circuit in Fig. 1c, equations (6a) and (6b) are obtained for the AVDM assuming M_1 = M_4, M_2 = M_5 and M_3 = M_6, and where $I_{oDM_m} = I_{sp}\frac{W_3}{L_3}e^{\frac{-|V_{i1}-V_{i2}|+V_{th3}}{nV_T}}$ is the output current of the SSF branch with the higher input voltage. Equation (6a) applies when both M_3 and M_6 are in weak inversion while (6b) applies when either M_3 or M_6 are in strong inversion.

$$I_{oABS} = \begin{cases} I_{sp}\frac{W_3}{L_3}e^{\frac{|V_{i1}-V_{i2}|+V_{th3}}{nV_T}} + I_{oDM_m} & \text{(6a)} \\ \frac{1}{2}\mu_p C_{ox}\frac{W_3}{L_3}(|V_{i1}-V_{i2}|+V_{th3})^2 + I_{oDM_m} & \text{(6b)} \end{cases}$$

When $V_{i1} = V_{i2}$, the output current I_{oABS} achieves its minimum value, and can be calculated as twice the subthreshold current of M_3 when the source-voltage is equal to zero, (7).

$$I_{oABS}|_{V_{i1}=V_{i2}} = 2 \times I_{sp}\frac{W_3}{L_3}e^{\frac{V_{th3}}{nV_T}} \tag{7}$$

III. Low-power LDO with adaptive biasing error amplifier

In a conventional LDO the two inputs of the EA are set to practically the same voltage level due to the feedback action. Sudden changes in the load current cause a rapid variation of the LDO output voltage, thus unbalancing the EA input voltages. The time response of the output voltage depends on the capability to drive the pass transistor and, hence, on the maximum output current of the EA. Therefore, it would be advisable to use an EA featuring a class AB behavior, with a high output current during transient periods, to properly drive the pass transistor, along with a reduced biasing current in the steady state regime, to ensure a low quiescent power consumption.

Fig. 2 shows the schematic of the proposed adaptively biased error amplifier. It consists of three blocks. The left part of the circuit is the SSF absolute voltage difference meter plus some additional biasing circuitry, the central part is a block that determines the biasing point of the amplifier, and the right section is a folded-cascode amplifier with a PMOS input pair. In the AVDM part, the transistors $M_{biasSSF}$, M_{PbSSF} and M_{NbSSF} are used to determine the biasing currents of the SSFs in the circuit, I_{bias1} and $I_{bias1} + I_{bias2}$, by means of the current mirrors $M_{biasSSF} - M_{PSSF+,PSSF-}$ and $M_{NbSSF} - M_{NSSF+,NSSF-}$, respectively, generated from an external bias current $I_{biasSSF}$. The output current of the voltage difference meter, I_{oABS}, is mirrored to the next part of the circuit by the transistor $M_{absdiff}$ and its gate voltage V_Δ. Then, the biasing circuit translates the output current of the absolute voltage difference meter to the bias point of the amplifier. The size ratio $M_{mirror} : M_{absdiff}$ determines the bias current of the amplifier $I_{biasAMP}$, and then $I_{biasAMP}$

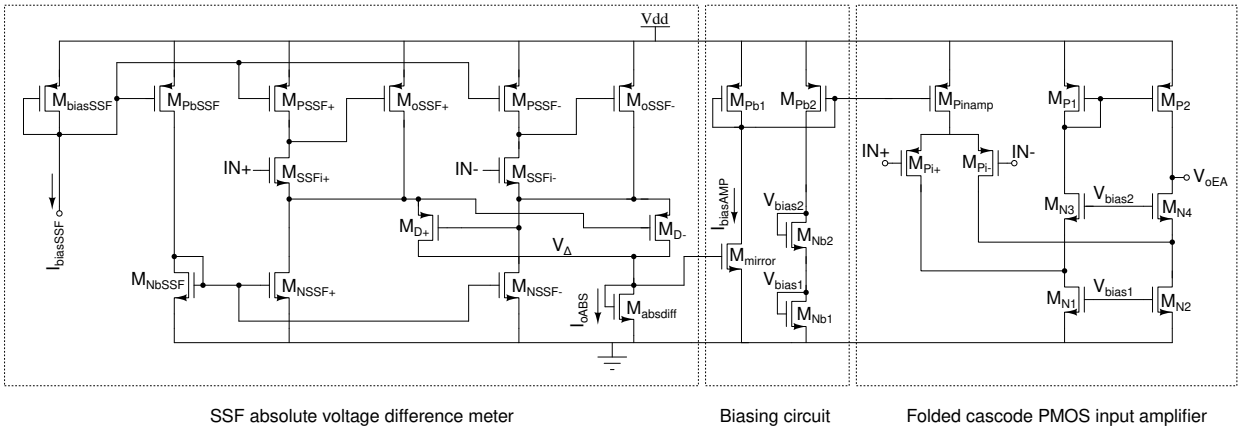


Fig. 2: Proposed adaptively biased error amplifier.

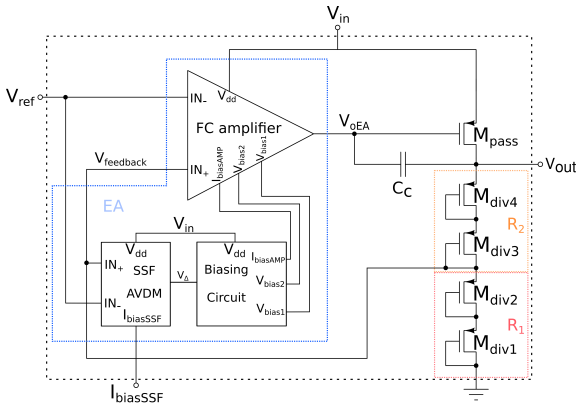


Fig. 3: LDO with adaptively biased error amplifier.

is mirrored to M_{Pb1} and M_{Pinamp} to generate the voltages V_{bias1} and V_{bias2} that bias the cascode stage and to bias the differential pair M_{Pi+}, M_{Pi-} respectively. When the inputs IN_+ and IN_- have different values, I_{oABS} and $I_{biasAMP}$ will significantly increase, and therefore the error amplifier will be capable of providing a larger output current to charge or discharge its output node and consequently change the pass transistor gate voltage faster.

The implemented AVDM of the error amplifier has been designed to work in the subthreshold regime, using an input biasing current, $I_{biasSSF}$, as low as 100 pA. Besides, the channel dimensions of transistors M_{oSSF+} and M_{oSSF-} have been set with a small W/L ratio in order to limit the maximum output current to hundreds of nA.

The implemented LDO is shown in Fig. 3. A low quiescent current in the output branch would require values in the order of the GΩ for a passive feedback network. For this reason, diode-connected transistors $M_{div,i}$, with i = 1 to 4, are used. Indeed, they are sized so that their equivalent resistance is so high that their leakage current is as low as 400 pA. If $M_{div,i}$ transistors are identically sized, the expected output voltage of the LDO, V_{out}, will be equal to $2V_{ref}$.

Fig. 4a shows the simulation results of the proposed adaptively biased error amplifier shown in Fig. 2 using $V_{dd} = 1.8$ V, $I_{biasSSF} = 100$ pA and a fixed voltage $IN_- = 600$ mV. In this simulation the output current of the AVDM, I_{oABS}, and the biasing current of the amplifier, $I_{biasAMP}$, are shown as a function of the difference between the two input voltages, IN_+ and IN_-. As can be seen, $I_{biasAMP}$ varies from a minimum value of 105 pA, when both inputs are equal, to a maximum value of 7.3 μA, when the difference between IN_+ and IN_- is above 0.4 V.

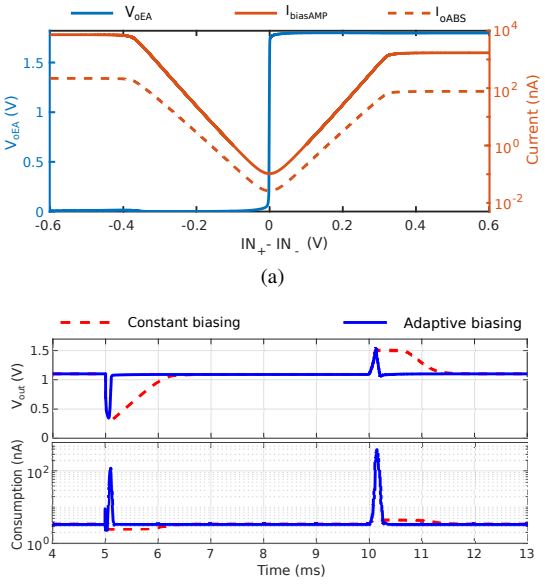
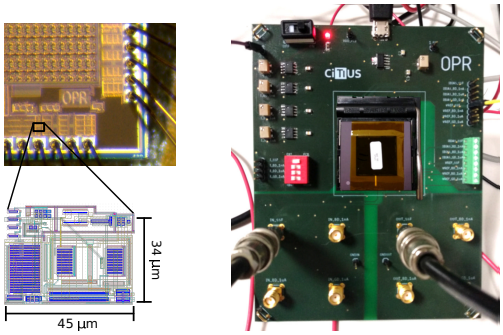


Fig. 4: (a) DC simulation of the error amplifier in Fig. 2. (b) Simulated transient response comparison between LDOs with and without the proposed adaptive biasing scheme.

In order to showcase the transient response improvement using the proposed adaptive biasing scheme, Fig. 4b shows a comparison between the proposed LDO with the adaptively biased error amplifier and an LDO with a fixed biasing current. The quiescent current considered in both cases is $I_Q \simeq 3.5$ nA. The simulation shows the transient response of both LDOs



(a) (b)

Fig. 5: (b) Chip microphotography indicating the circuit position and superimposed image of the layout. (b) Testing PCB.

for a step-up and a step-down transition of the output current from/to 4.4 nA to/from 3.83 mA at $t = 5$ ms and $t = 10$ ms, respectively. The step-up settling time, $t_{s,up}$, goes from 1.4 ms with the constant biasing method to 0.12 ms using the proposed adaptively biased error amplifier, which means a settling time improvement of 12×. For the step-down transition, $t_{s,down}$ goes from 1.44 ms to 0.22 ms, resulting in a 6.5× improvement for the proposed LDO.

IV. Experimental Results

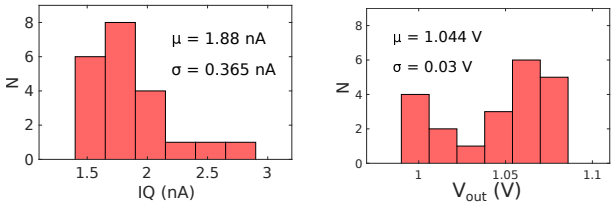
A proof-of-concept chip of the proposed LDO with SSF-based adaptive biasing was fabricated in standard TSMC 0.18 μm technology. Fig. 5a shows a microphotograph of the 3.2x1.6 mm^2 chip highlighting the position of the LDO circuit, which has a form factor of 1473 μm^2. The complete PCB test setup is shown in Fig. 5b. A Tektronix MDO4034C oscilloscope and a Keithley 2450 SMU were used for the visualization and measurement of the signals. A current divider circuit was implemented on-chip in order to generate an LDO biasing current of $I_{biasSSF} = 100$ pA. The current divider is composed of several current mirror stages and provides a combined current reduction factor of 68000.

A summary of the experimental results of the proposed circuit can be found in Table I. For the experimental determination of the quiescent current consumption, $V_{in} = 1.8$ V and $V_{ref} = 550$ mV were considered. The measured I_Q distribution of the fabricated chips is shown in Fig.6a, giving a value of only 1.88 ± 0.37 nA. To the best of our knowledge this is the lowest quiescent current consumption ever reported for an LDO, [6]. The output voltage under these conditions can be seen in Fig. 6b. The measured LDO's line sensitivity is $LS = 1.7$ mV/V, equivalent to 0.13% V between 1.15 V and 1.8 V. For the load regulation, an average value of LR $= 40.2 \pm 5.1$ mV/mA was obtained. This relatively large value is attributed to the impedance of the metal line connecting the circuit output to the pad of the chip, which has been calculated to be around 41.8 Ω based on both technology specifications and experimental estimation.

The transient response of the regulator is shown in Fig. 7. An analog switch was used to connect and disconnect a load resistance of $R_L = 269$ Ω to the output of the regulator, which is equivalent to alternate the load current from $I_L = 4.4$ nA, to $I_L = 3.86$ mA. Under these conditions, the average settling time was $t_{s,up} = 0.98 \pm 0.35$ ms for the step-up load current pulse and $t_{s,down} = 1.01 \pm 0.05$ ms in the step-down case. These settling times are significantly larger than the simulated values, which can be attributed to the large parasitic capacitance and resistance of the chip pads and lines corresponding to V_{in} and V_{out}, along with the input capacitance of the instrumentation.

TABLE I: Summary of the experimental results.

	This work	[6]
Technology	0.18 μm	65 nm low-leakage
Size	1473 μm^2	4200 μm^2
I_Q (nA)	1.88	30
LS (mV/V)	1.7	-
LR (mV/mA)	40.2	1.22
PSR (dB) 10 Hz	-48 @ 4.4nA -32 @ 3.86mA	-
PSR (dB) 10 kHz	-48 @ 4.4 nA -7 @ 3.86 mA	<-40 @ 10.3 mA



(a) (b)

Fig. 6: Distribution of the measured (a) quiescent current and (b) output voltage values for 22 chip samples.

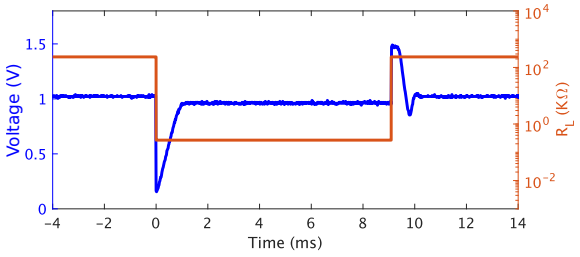


Fig. 7: Measured transient response of the proposed LDO.

V. Conclusions

An absolute voltage difference meter circuit based on the super source follower structure is presented and used to adaptively modify the biasing current of the error amplifier on a conventional capacitor-less LDO configuration. The experimental results show a quiescent current of only 1.88 nA with line sensitivity of 1.7 mV/V and load regulation of 40.2 mV/mA.

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