Doctoral Meeting: 'Using hardware counter data to model performance and energy usage in NUMA systems'

Data: venres, 15 febreiro, 2019 - 12:00 - 13:30

Lugar: CiTIUS Assembly Hall

Poñente(s): Miguel López Becoña (CiTIUS predoctoral researcher)

Idioma: Inglés

Streaming: Non

Multicore systems present on-board memory hierarchies and communication networks that influence performance when executing shared-memory parallel codes. Characterising this influence is complex, and understanding the effect of particular hardware configurations on different codes is of paramount importance.

In this thesis, hardware counters are used to model energy usage in the machine and characterise the behavior of each running thread of a parallel code. These hardware counters are monitoring mechanisms included in the Performance Monitoring Unit (PMU) of the majority of microprocessors, and its use is gaining popularity as an analysis and validation tool. This technology provides high accuracy with a low overhead.

This information can be used by a scheduler to balance the workloads, guiding thread and page migration strategies in order to increase data locality and affinity, and finally lead to power saving and performance optimization in multithreaded applications.