Variability studies in advanced digital semiconductor devices

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Outline

- Motivation
- Simulation methodology
- Results
- Conclusion

Outline

- Motivation → Why is our research relevant ?
- Simulation methodology
- Results
- Conclusion

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Outline

- Motivation → Why is our research relevant ?
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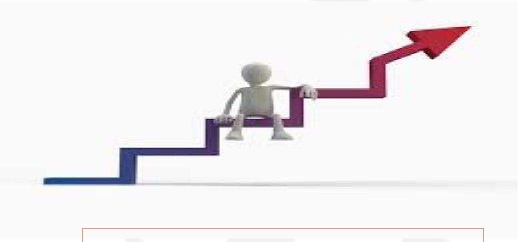

Step-by-step

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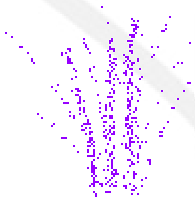
Outline

- Motivation → Why is our research relevant ?
- Simulation methodology → How do we do it?
- Results → Focus on variability studies
- Conclusion

Outline

- Motivation → Why is our research relevant ?
- Simulation methodology → How do we do it?
- Results → Focus on variability studies
- Conclusion → Hurrah! It's over



Motivation

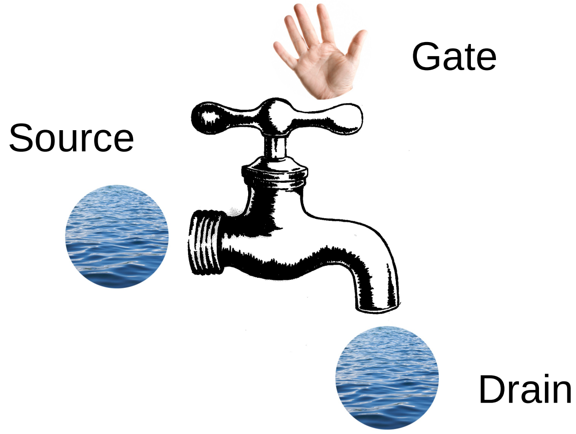
- What is a transistor?
- The scale of things
- Technology roadmap
- Collaborators and competitors

What is a transistor?

Picture a water tap

What is a transistor?

Picture a water tap



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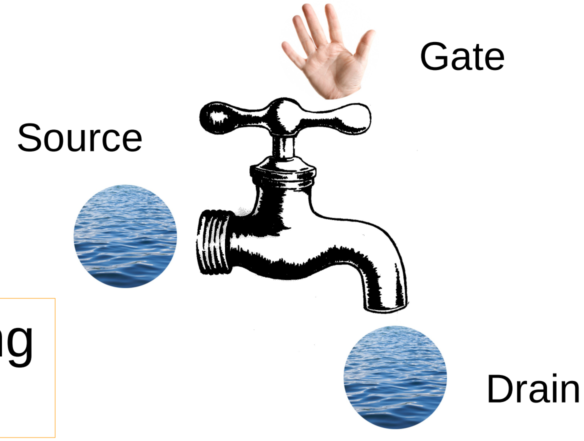
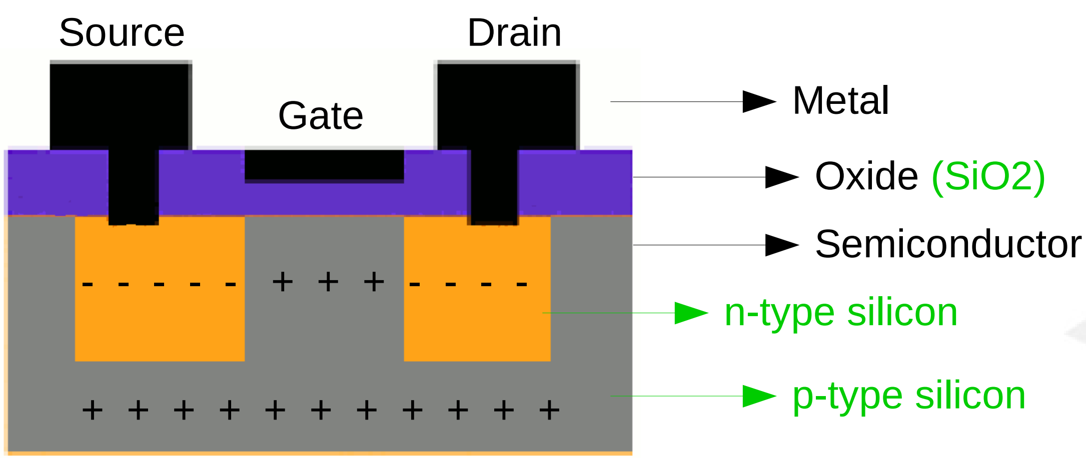


All transistors work by controlling the movement of carriers

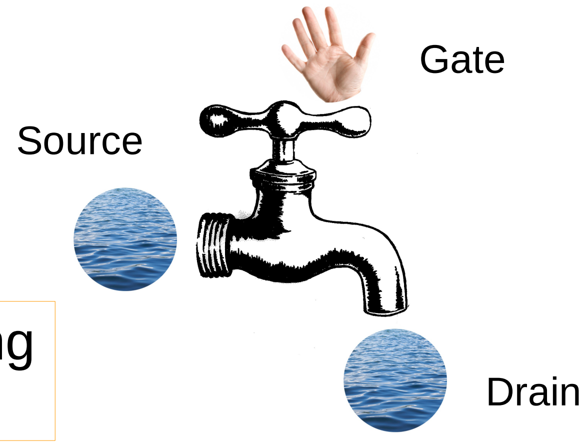


OFF

MOSFET transistor

What is a transistor?

Picture a water tap



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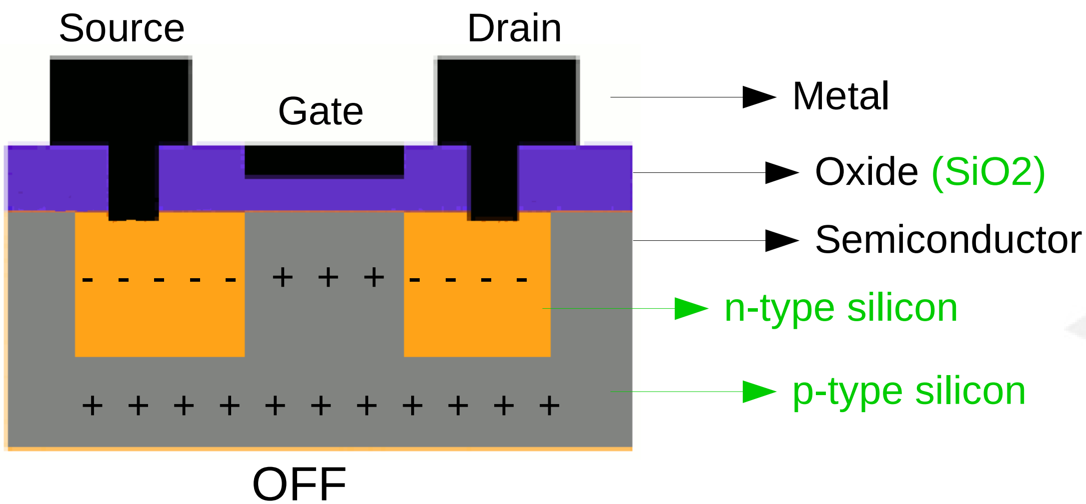
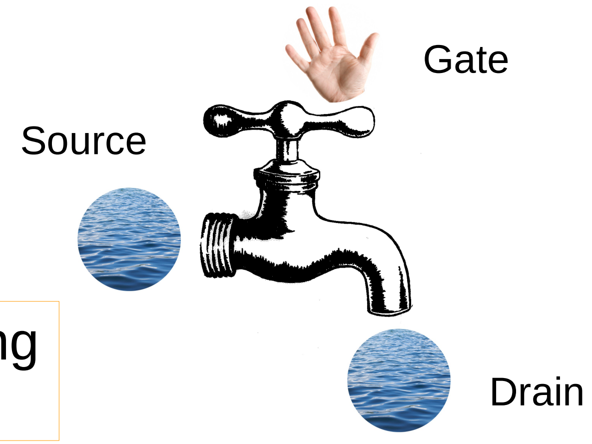


Cheap
Widely availabe
Easy to manufacture

MOSFET transistor

What is a transistor?

Picture a water tap



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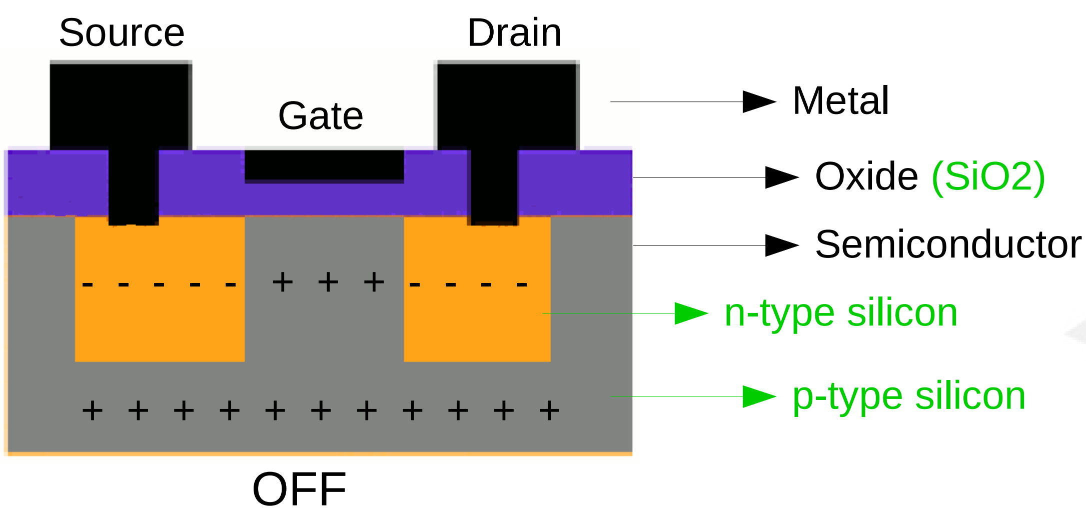

Isolation
Avoid current flow through the gate

Cheap
Widely availabe
Easy to manufacture

MOSFET transistor

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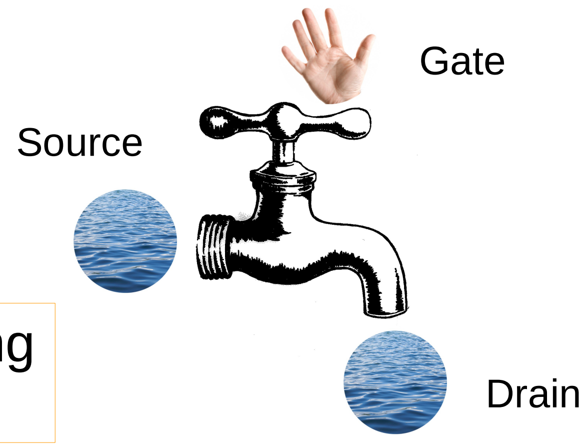
What is a transistor?

Picture a water tap



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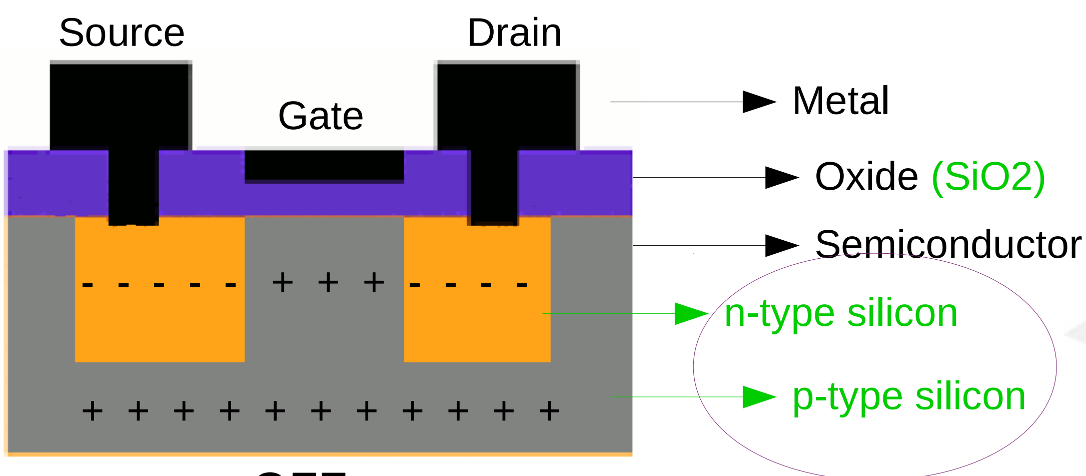


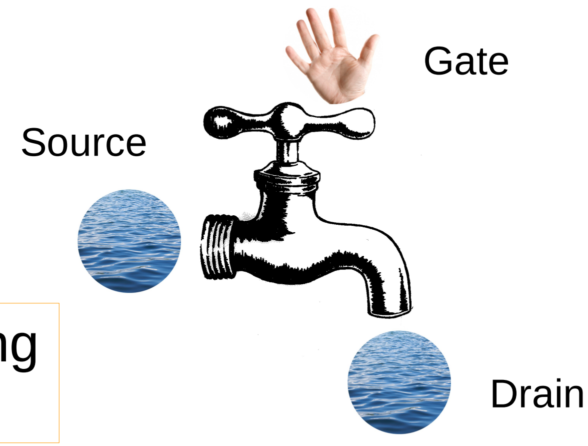
OFF

Add impurities (doping) to create carriers

MOSFET transistor

What is a transistor?

Picture a water tap



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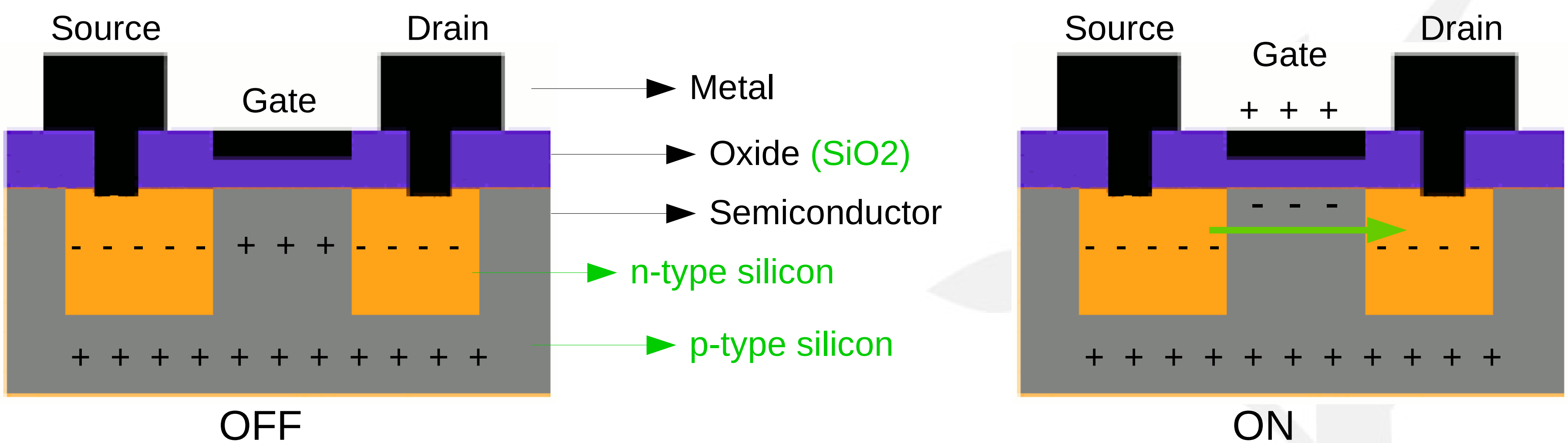

MOSFET transistor

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The scale of things

How small are we talking about?

Picture an ant

The scale of things

How small are we talking about?

Picture an ant

The scale of things

How small are we talking about?

Picture an ant

~ 5 mm

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The scale of things

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Grab a strand of your hair

The scale of things

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How small are we talking about?

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Grab a strand of your hair

~ 60-120 μm wide

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Red Blood cell

CiTIUS

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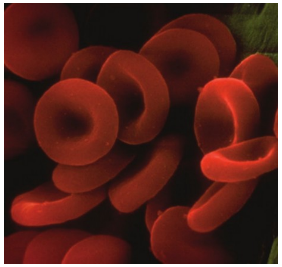

CiTIUS

The scale of things

How small are we talking about?

Picture an ant

~ 5 mm

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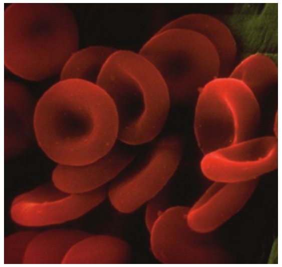

~ 7-8 µm

CiTIUS

The scale of things

How small are we talking about?

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~ 5 mm

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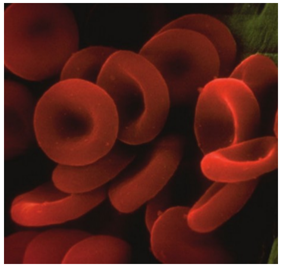
~ 60-120 µm wide

Red Blood cell



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FinFET device (state of the art)

CiTIUS

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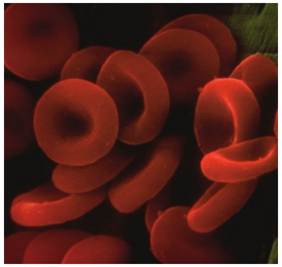

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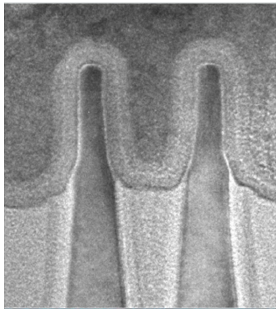

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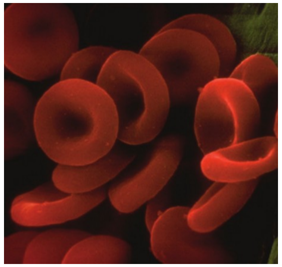

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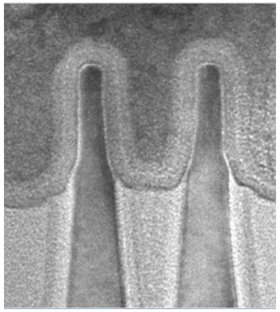

~ 10 nm gate length

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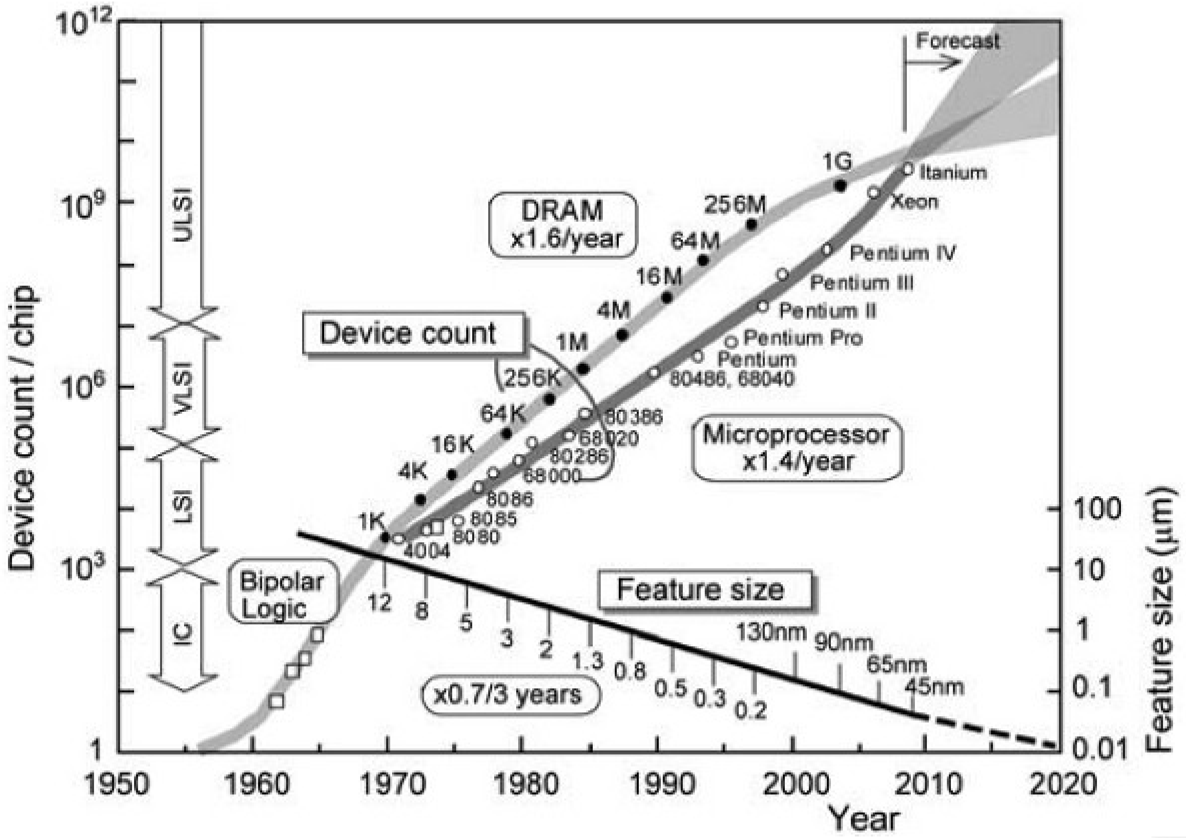
Transistors in an integrated circuit

How many?



Last **40 years**: more than **one-million fold increase** in the **device count** leading to almost the same increase in **processor performance**.

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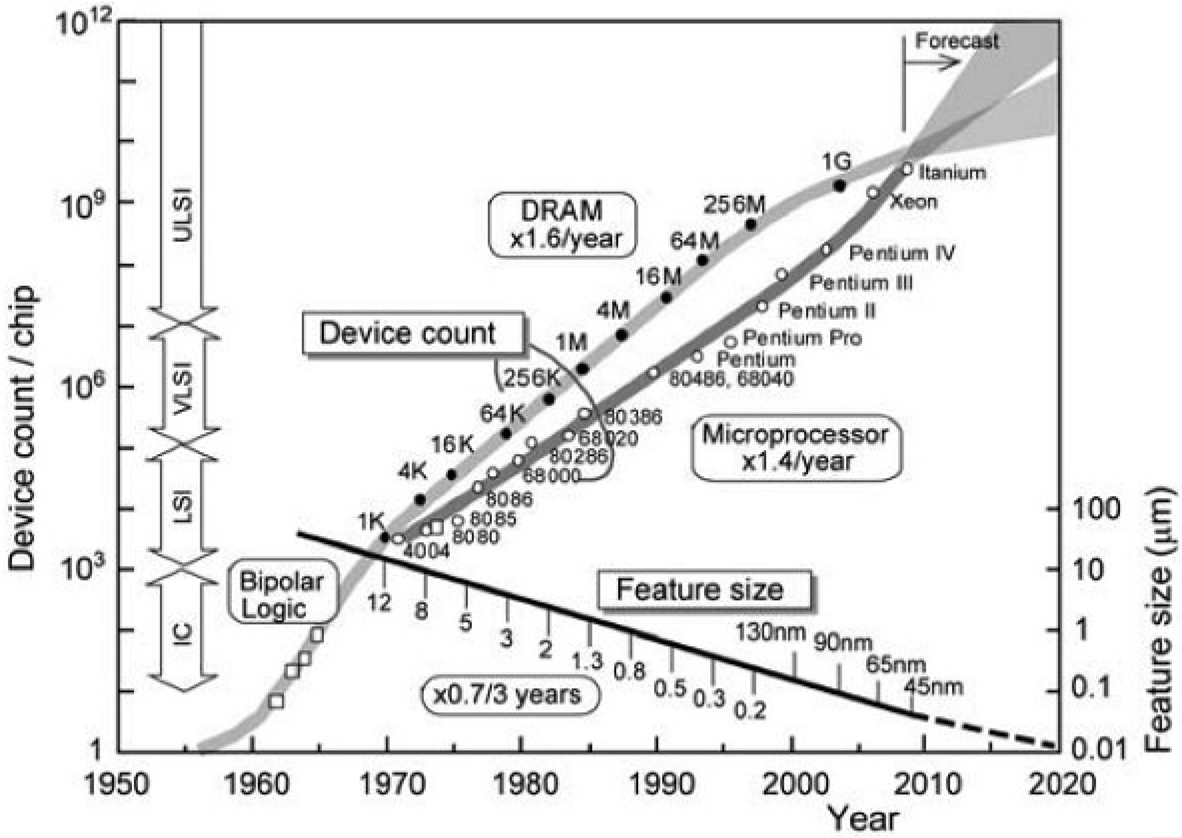
Transistors in an integrated circuit

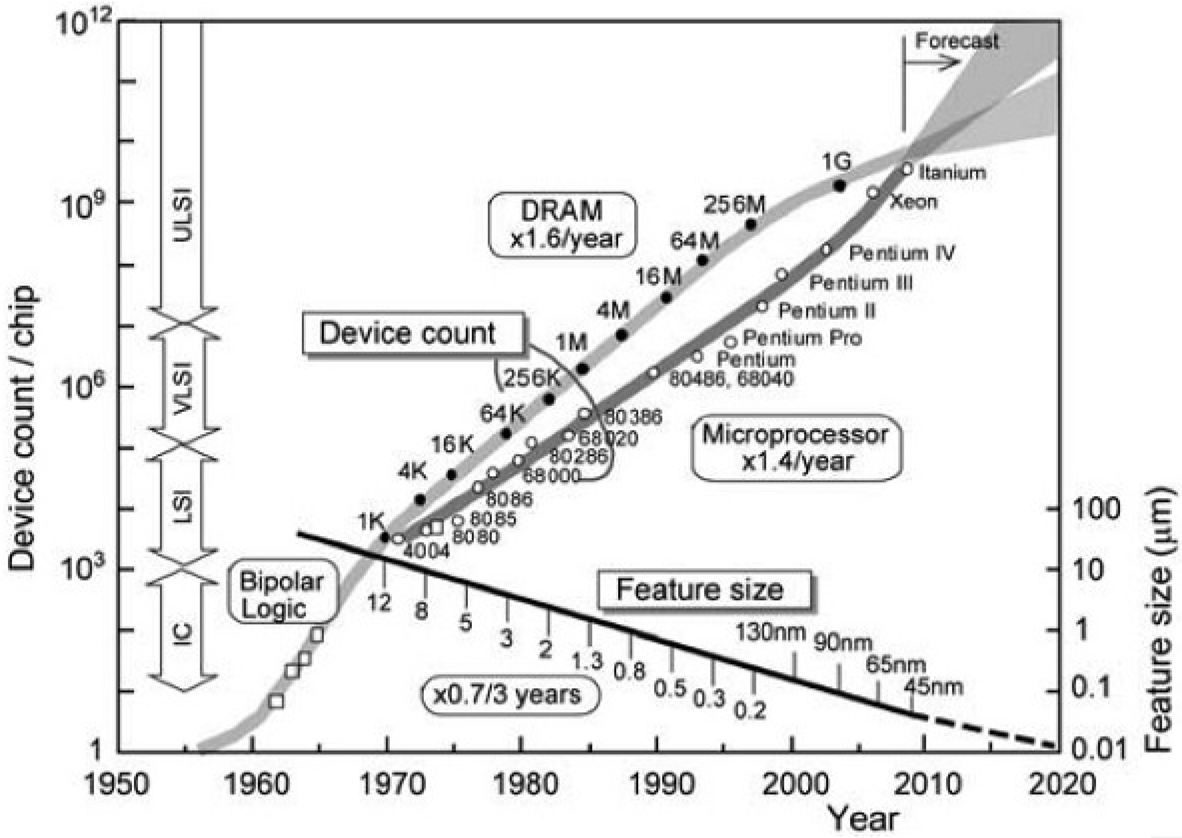
How many?



This explains the enormous development of **electronics** and **information technology**

Transistors in an integrated circuit

How many?



Example: Intel's 10-core Core i7 Broadwell-E processor has 3,200,000,000 **transistors** (**2016**, using 14 **nm** technology)

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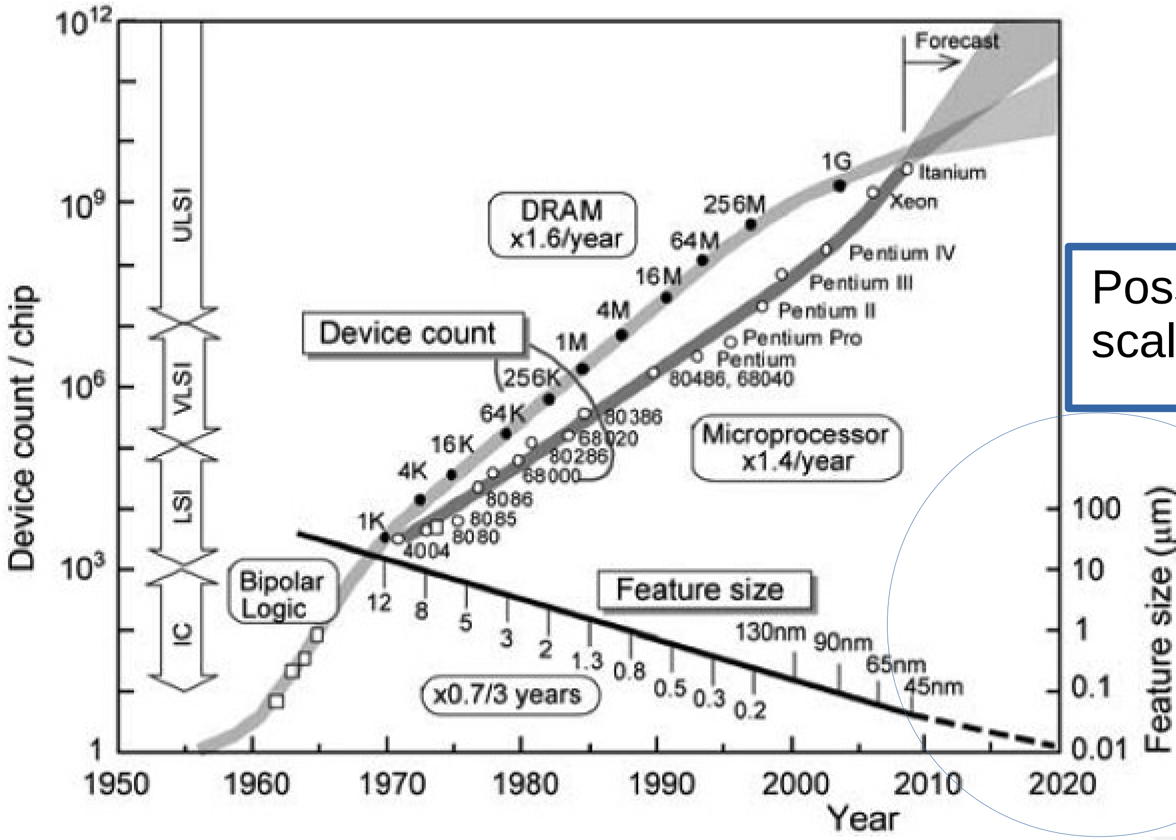
Transistors in an integrated circuit

How many?



Possible thanks to the scaling of the devices

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Transistors in an integrated circuit

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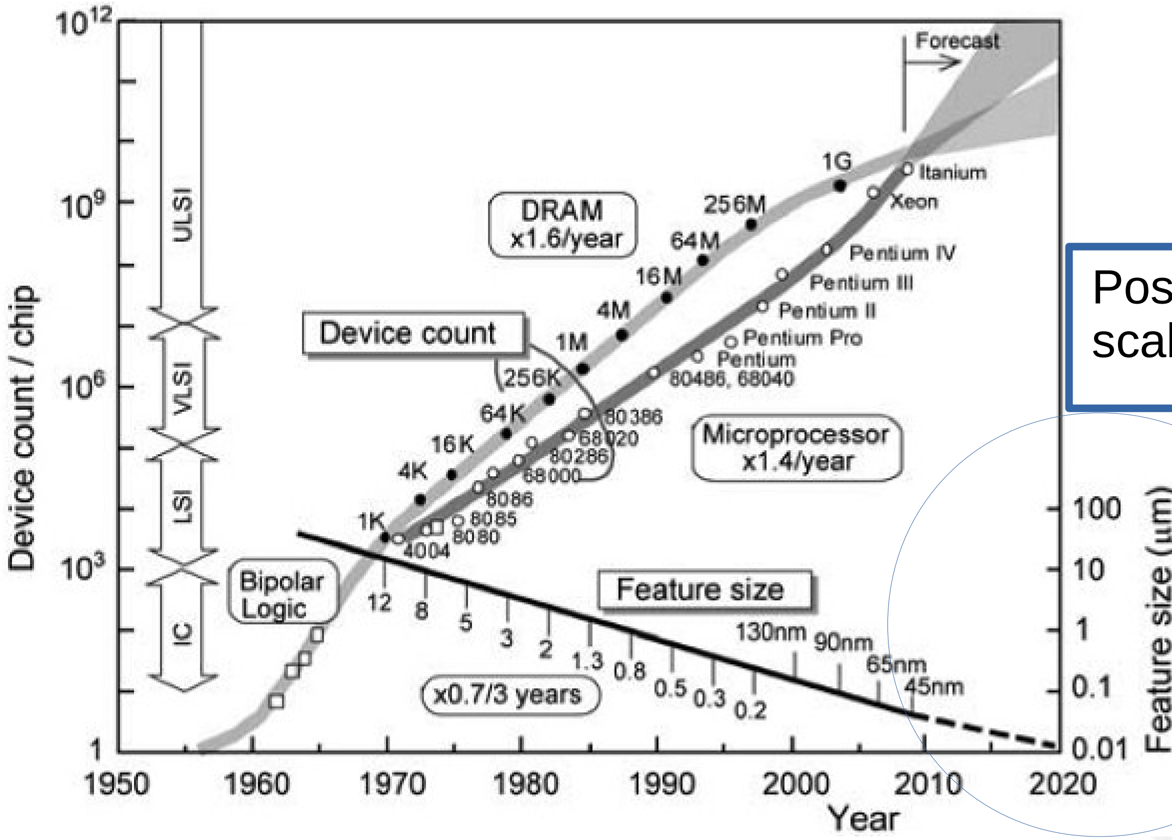


Possible thanks to the scaling of the devices

Nanometre regime

Example: Intel's 10-core Core i7 Broadwell-E processor has 3,200,000,000 **transistors** (**2016**, using 14 **nm** technology)

Technology roadmap

Evolution

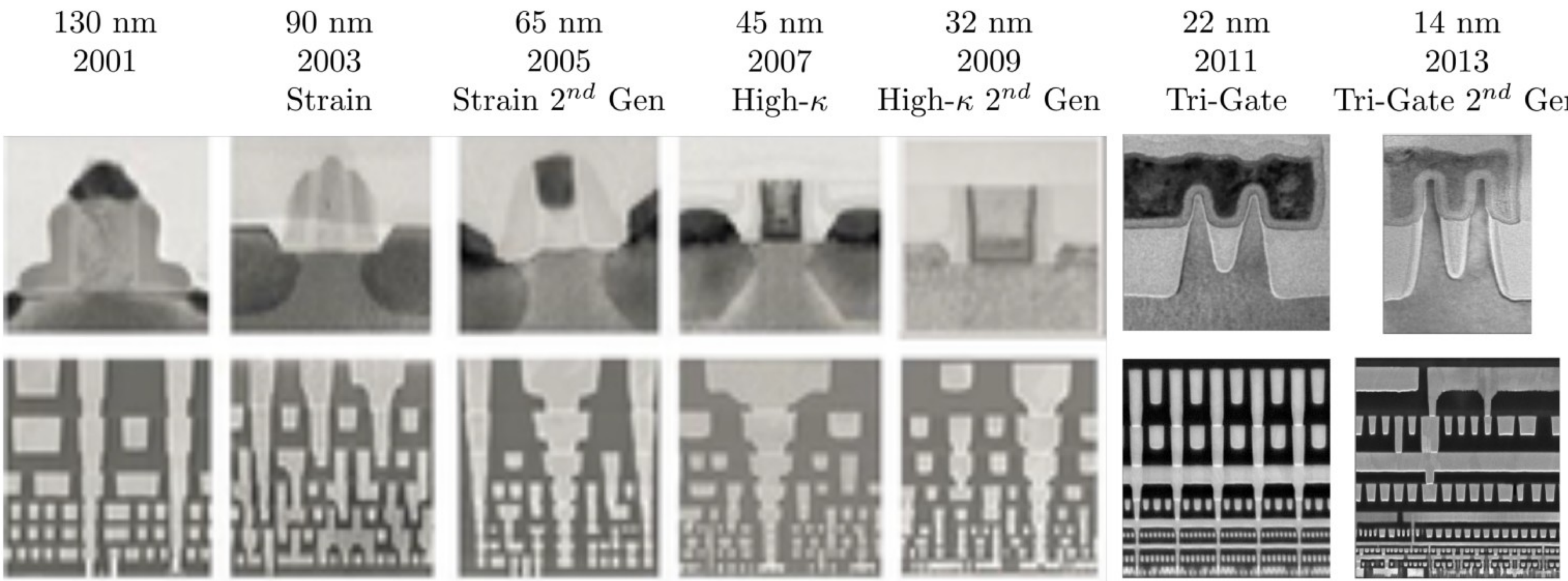
What is the consumer demand?

What is the consumer demand?

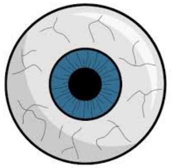
- **Faster** devices
- **Reduced power** consumption (mobile)
- **Ultra low power** consumption (IOT)

Technology roadmap

Evolution



Scaling has driven **device performance**
New technologies inserted frequently in the last 10 years
Devices will continue to **evolve** through further **innovation**



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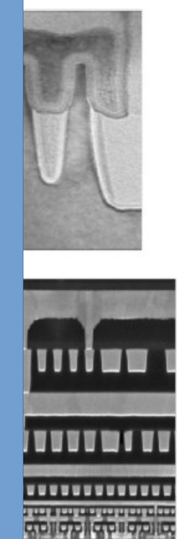
Technology roadmap

Evolution

130 nm
2001

AMD, NASDAQ evolution 2007-2010

4 nm
2013
te 2^{nd} Gen

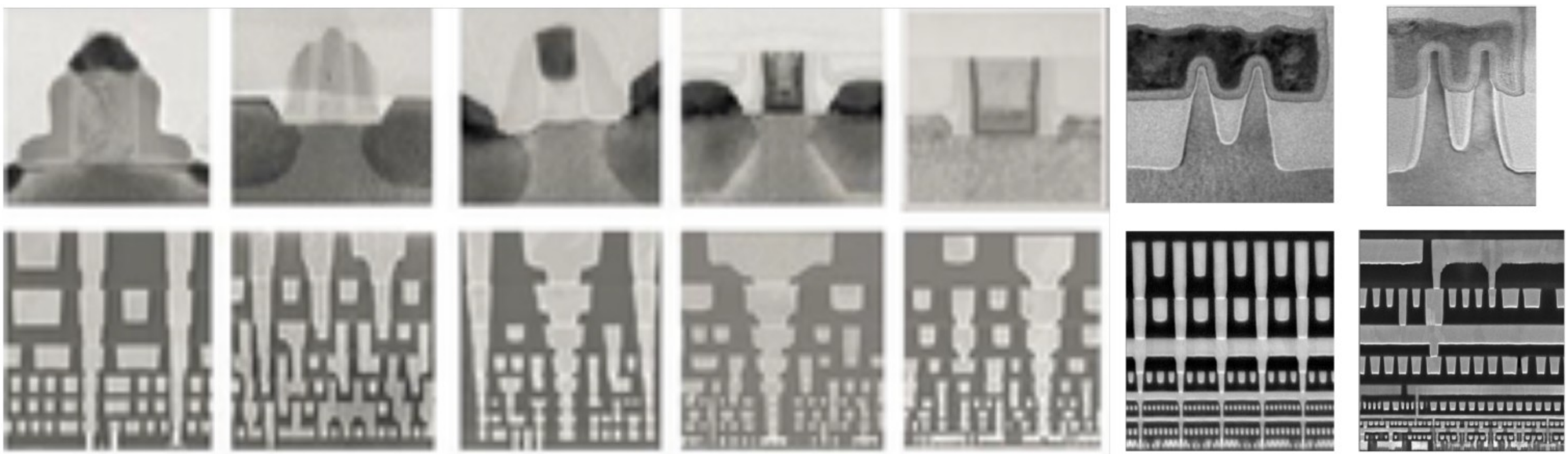


Technology roadmap
Evolution

PLANAR DEVICES

NON-PLANAR DEVICES

130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	14 nm
2001	2003	2005	2007	2009	2011	2013
	Strain	Strain 2^{nd} Gen	High-κ	High-κ 2^{nd} Gen	Tri-Gate	Tri-Gate 2^{nd} Gen



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Technology roadmap

Future predictions

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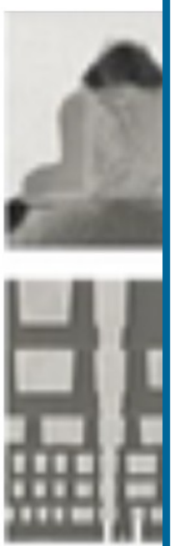
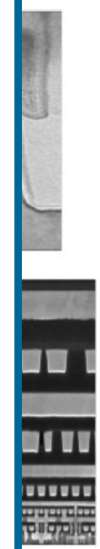
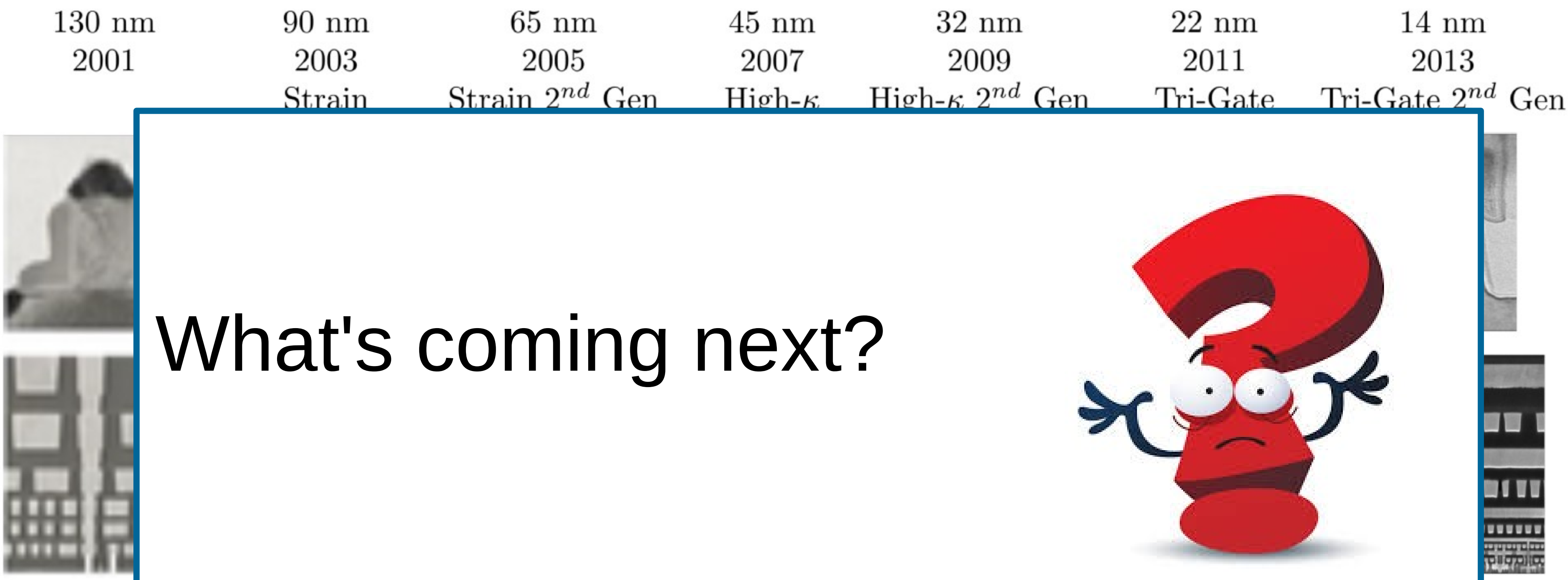






What's coming next?

Technology roadmap

Future predictions

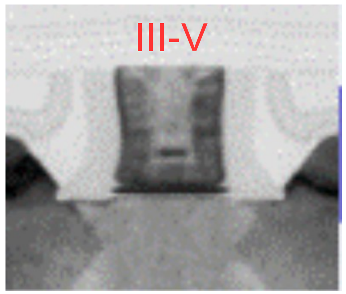
45 nm
2007
High-κ

32 nm
2009
High-κ 2nd Gen

22 nm
2011
Tri-Gate

14 nm
2013
Tri-Gate 2nd Gen

Material change

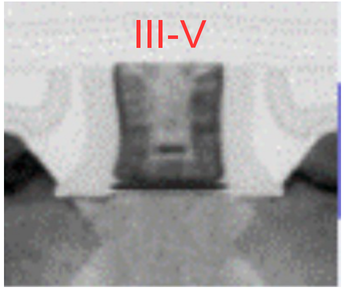


What's coming next?

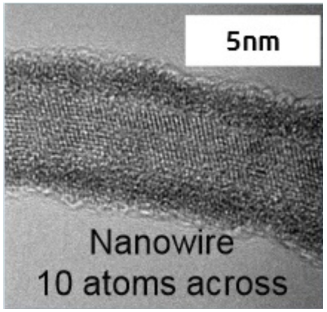
Technology roadmap

Future predictions

Material change



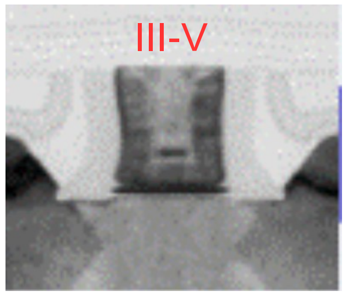
New architectures



What's coming next?

Technology roadmap
Future predictions

Material change



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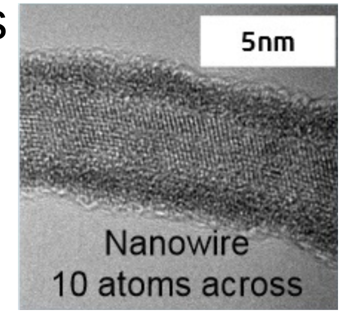
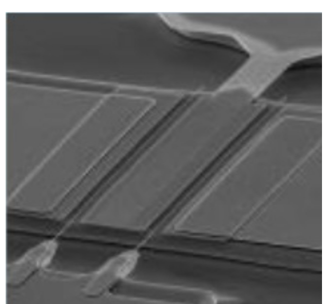


14 nm
2013
ri-Gate 2^{nd} Gen

What's coming next?

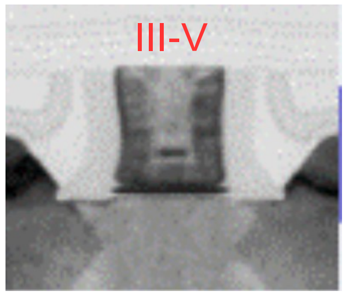
Quantum devices



Technology roadmap

Future predictions

Material change



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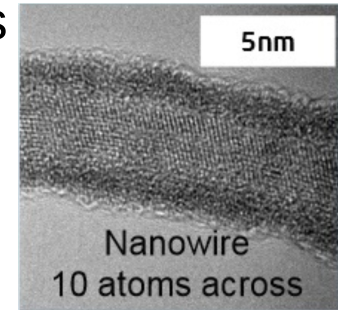

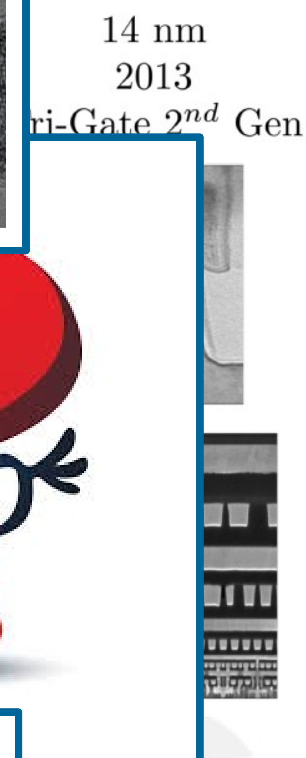

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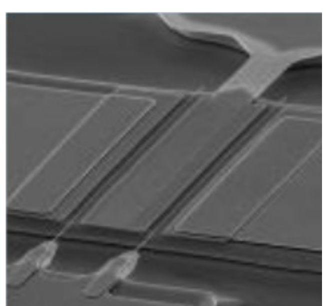
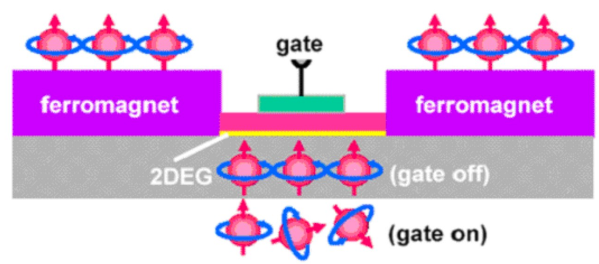


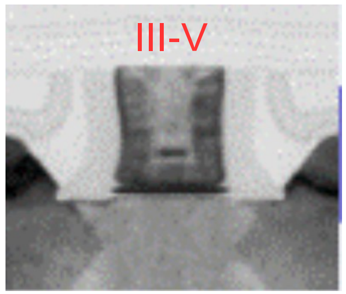
Spintronics



Technology roadmap

Future predictions

Material change



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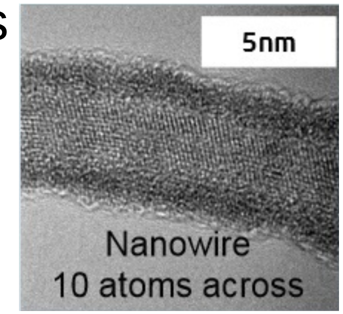
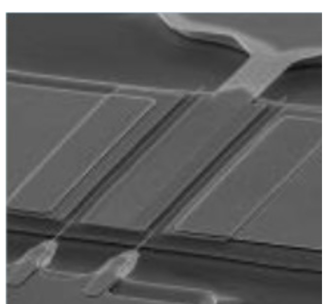


14 nm
2013
ri-Gate 2^{nd} Gen

Graphene

What's coming next?

Quantum devices



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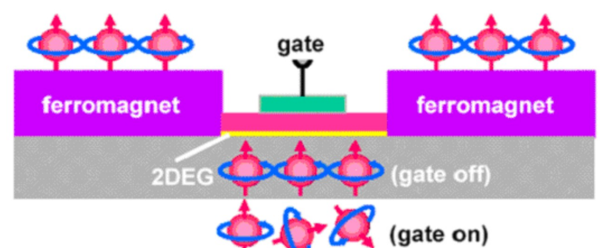

Technology roadmap
Future predictions

14 nm
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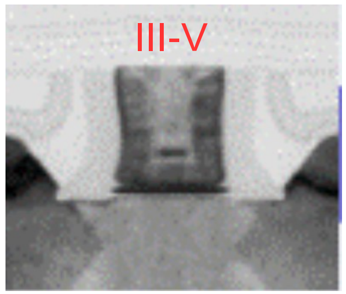
Material change



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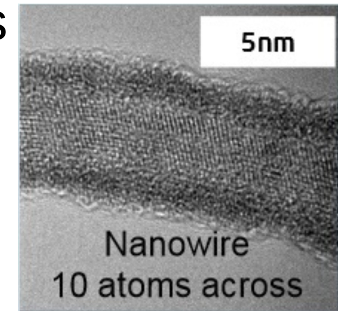
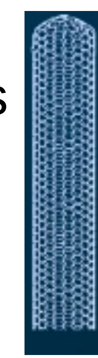


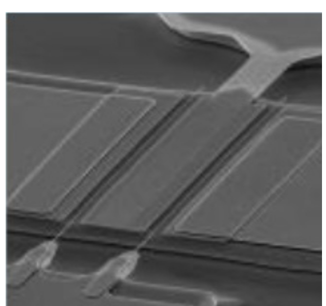
What's coming next?

Graphene

Carbon nanotubes



Quantum devices



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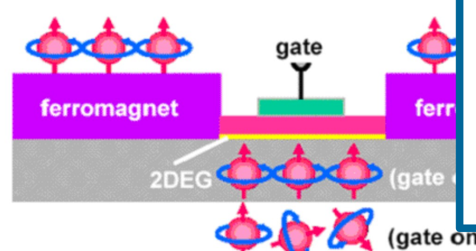


Apple iPhone 6s Smartphone

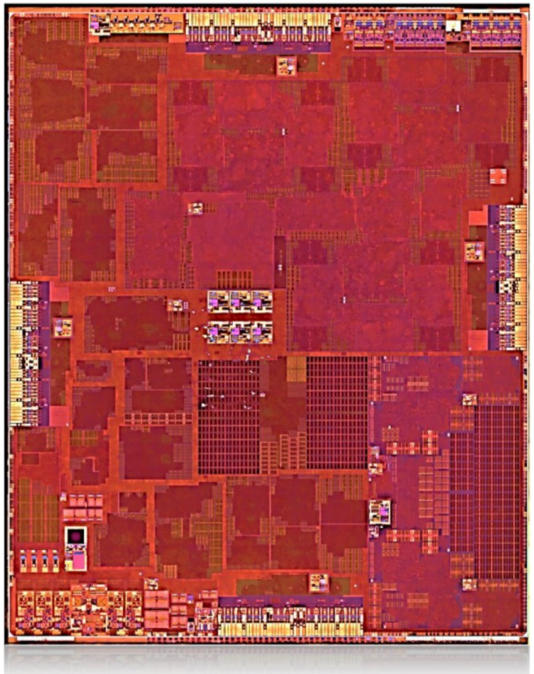
What's inside?

Example of **Low Power** and **High Performance** application.

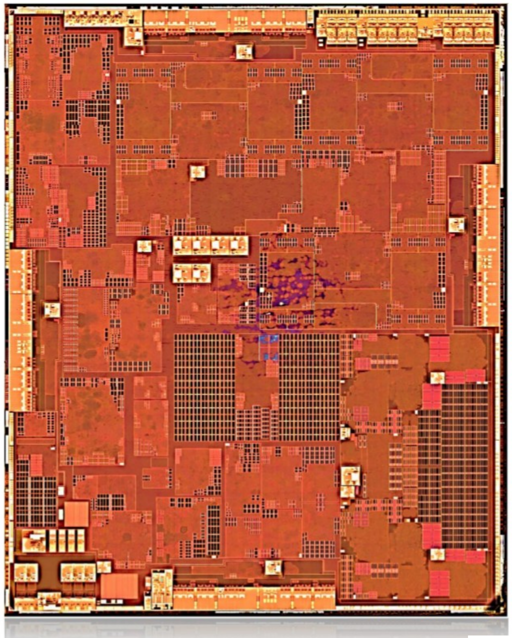
CiTIUS

Apple iPhone 6s Smartphone

What's inside?



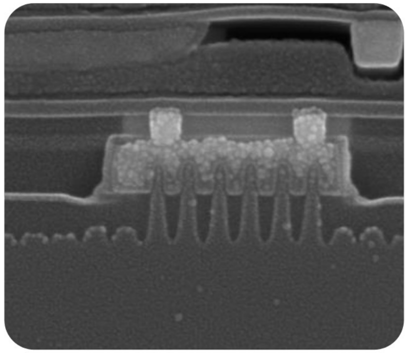
APL1022 TSMC 16 nm FinFET



APL0898 Samsung 14 nm FinFET

Apple has dual sourced its **Processor** from **Samsung** (14 nm FinFET) and **TSMC** (16 nm FinFET).

Example of **Low Power** and **High Performance** application.



TSMC 16 nm FinFET

Collaborators and competitors

Who is who?

UNIVERSIDAD DE GRANADA

Prifysgol Abertawe
Swansea University

UAB
Universitat Autònoma de Barcelona

IμE

ETH zürich

Collaborators and competitors

Who is who?

nanoHUB

University of Glasgow

Gold Standard Simulations

SYNOPSYS®

Silicon to Software™

SILVACO

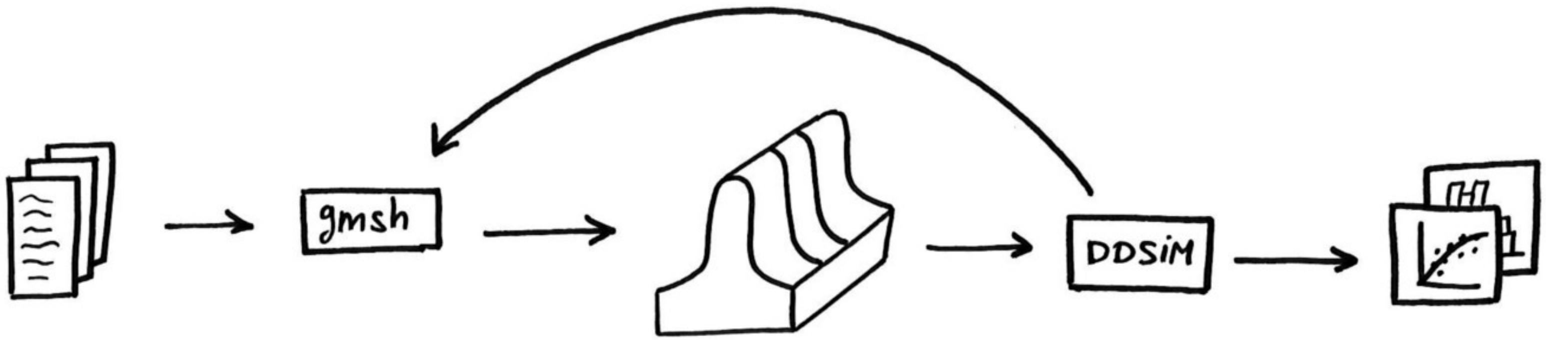
Outline

- Motivation
- **Simulation methodology**
- Results
- Conclusion

Simulation methodology

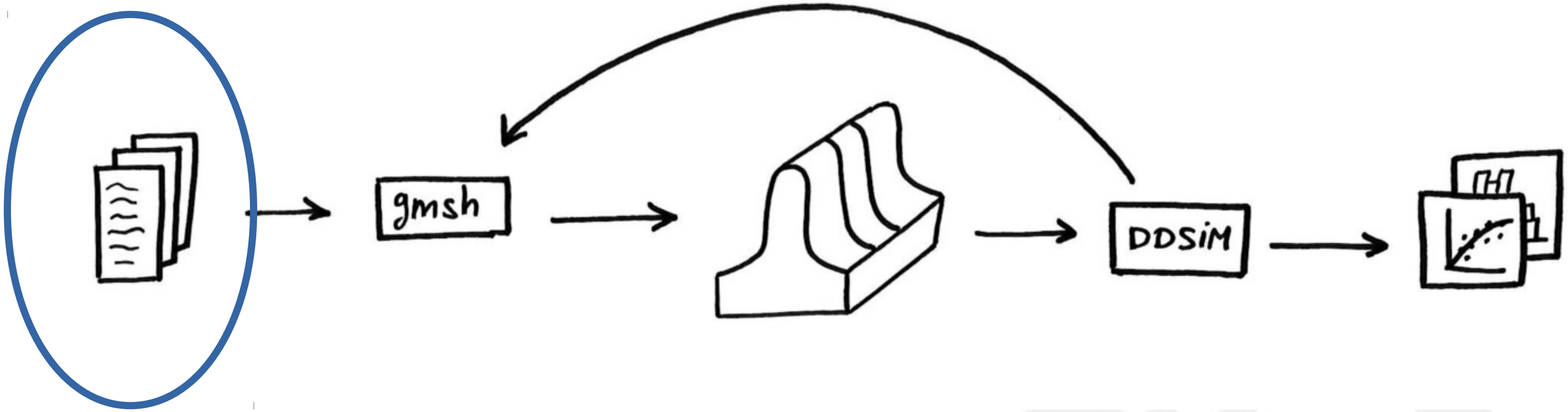
- Device selection
- Device creation
- Pre-processing stage
- Simulation of the device
- Analysis of the results

Simulation pipeline



CiTIUS

Simulation pipeline



Device selection

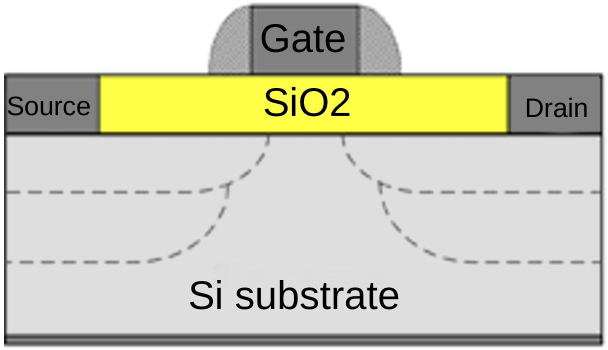
Device selection

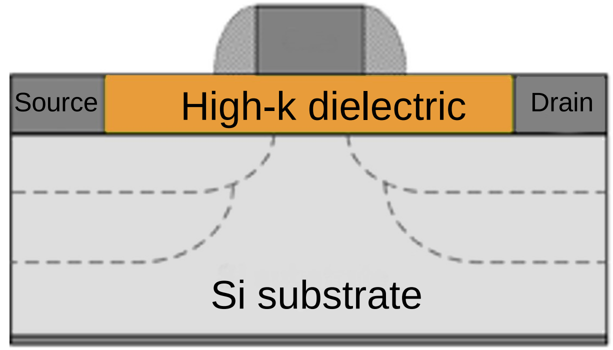
Sources of information

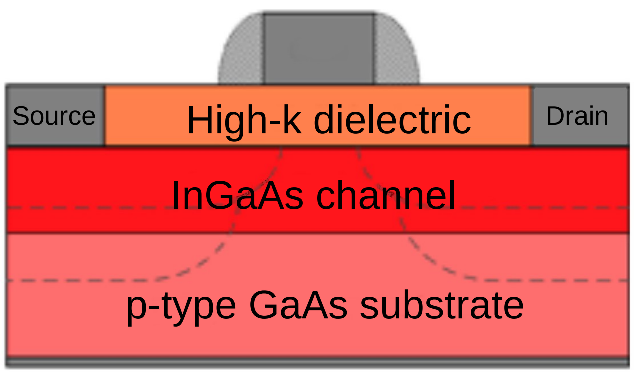
- Experimental data
- ITRS (International Technology Roadmap for Semiconductors)
- Scientific papers

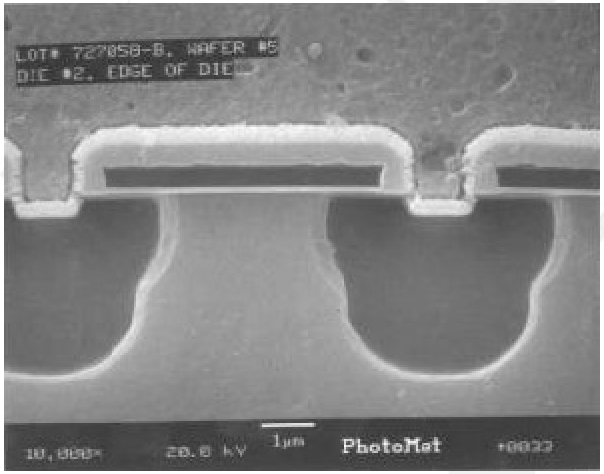
Device selection

50 nm gate length MOSFET









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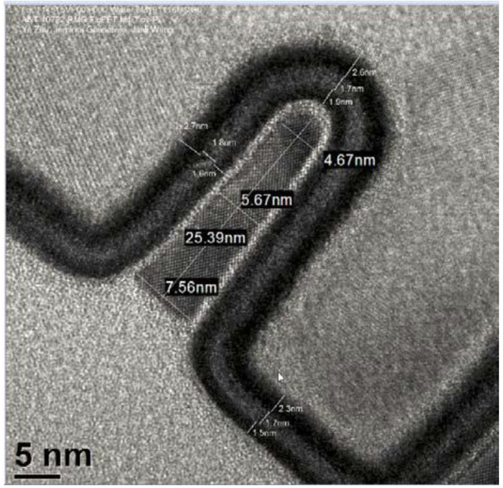
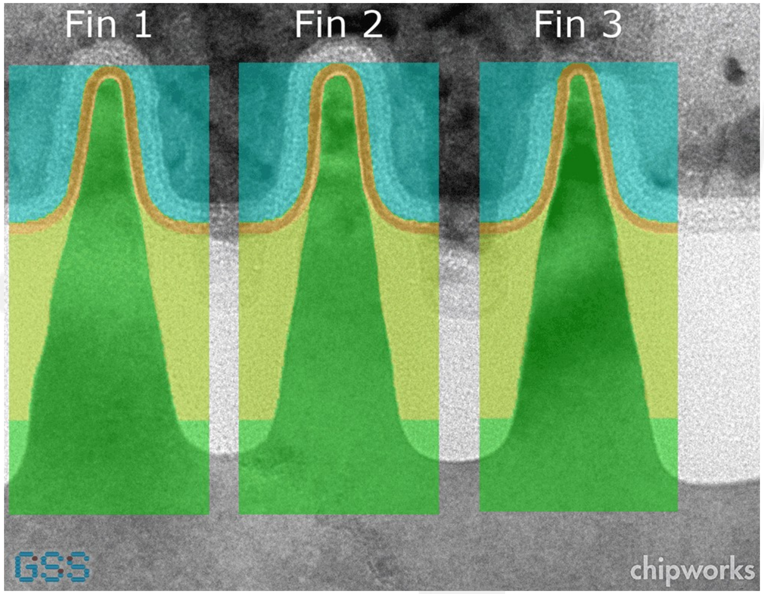
Device selection

10.7 nm gate length Si FinFET

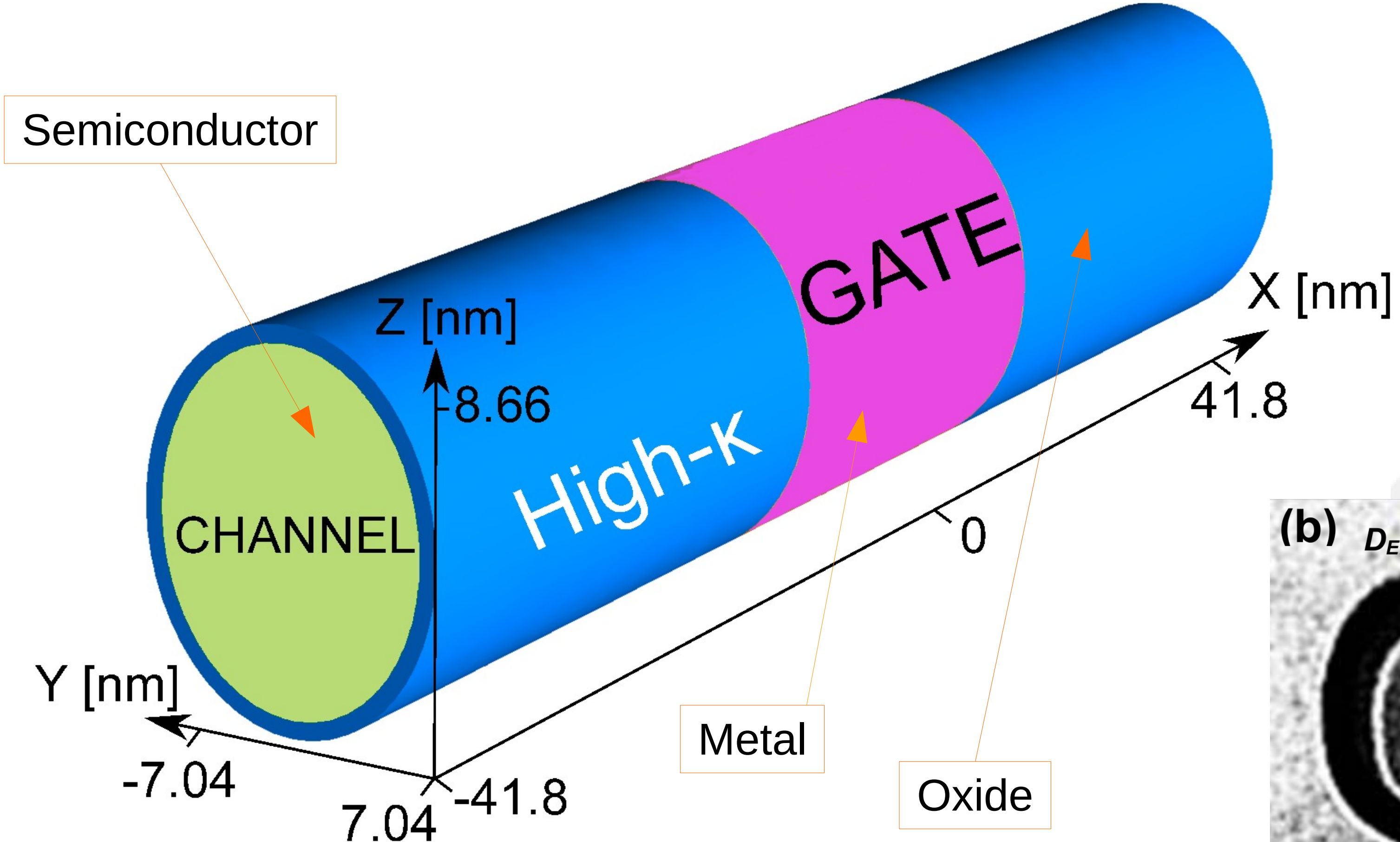


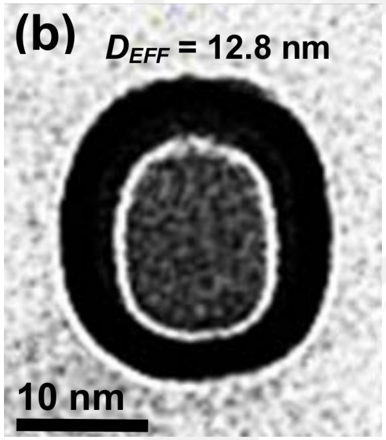


CiTIUS

Device selection

22 nm gate length Si GAA NW FET

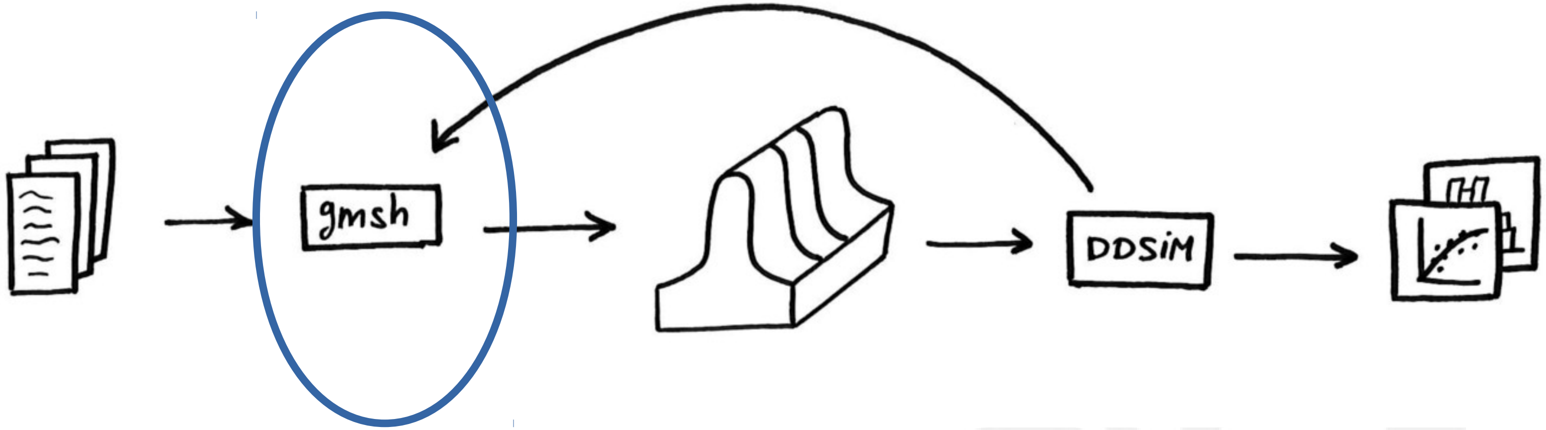




(b) S Bangsaruntip, et al. *Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond*. **IEDM Tech. Dig**. pp.526-9, 2013. (IBM Research Division)

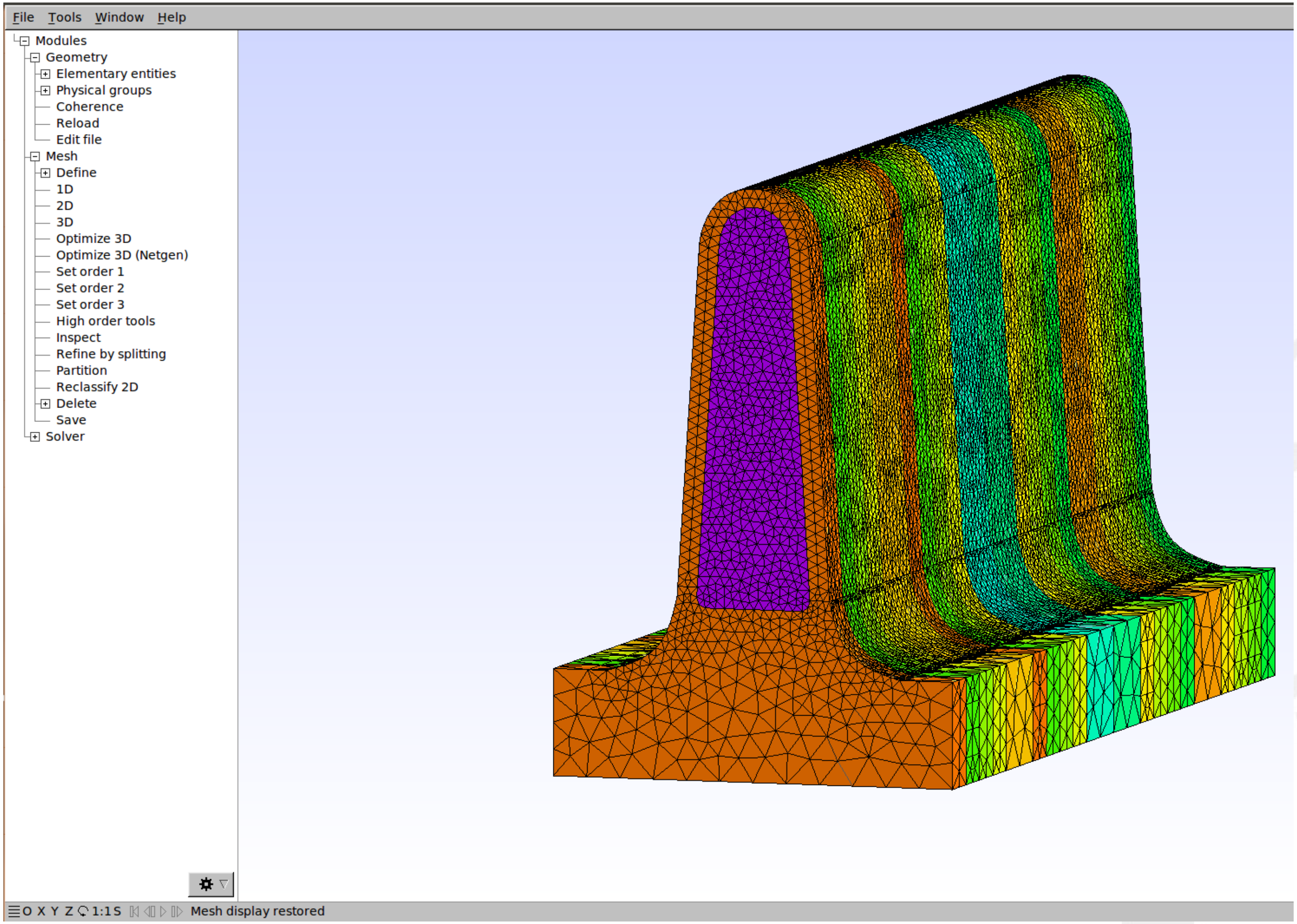
CiTIUS

Simulation pipeline



Device creation

GMSH: 3D finite element mesh generator
Screenshot



GMSH: 3D finite element mesh generator

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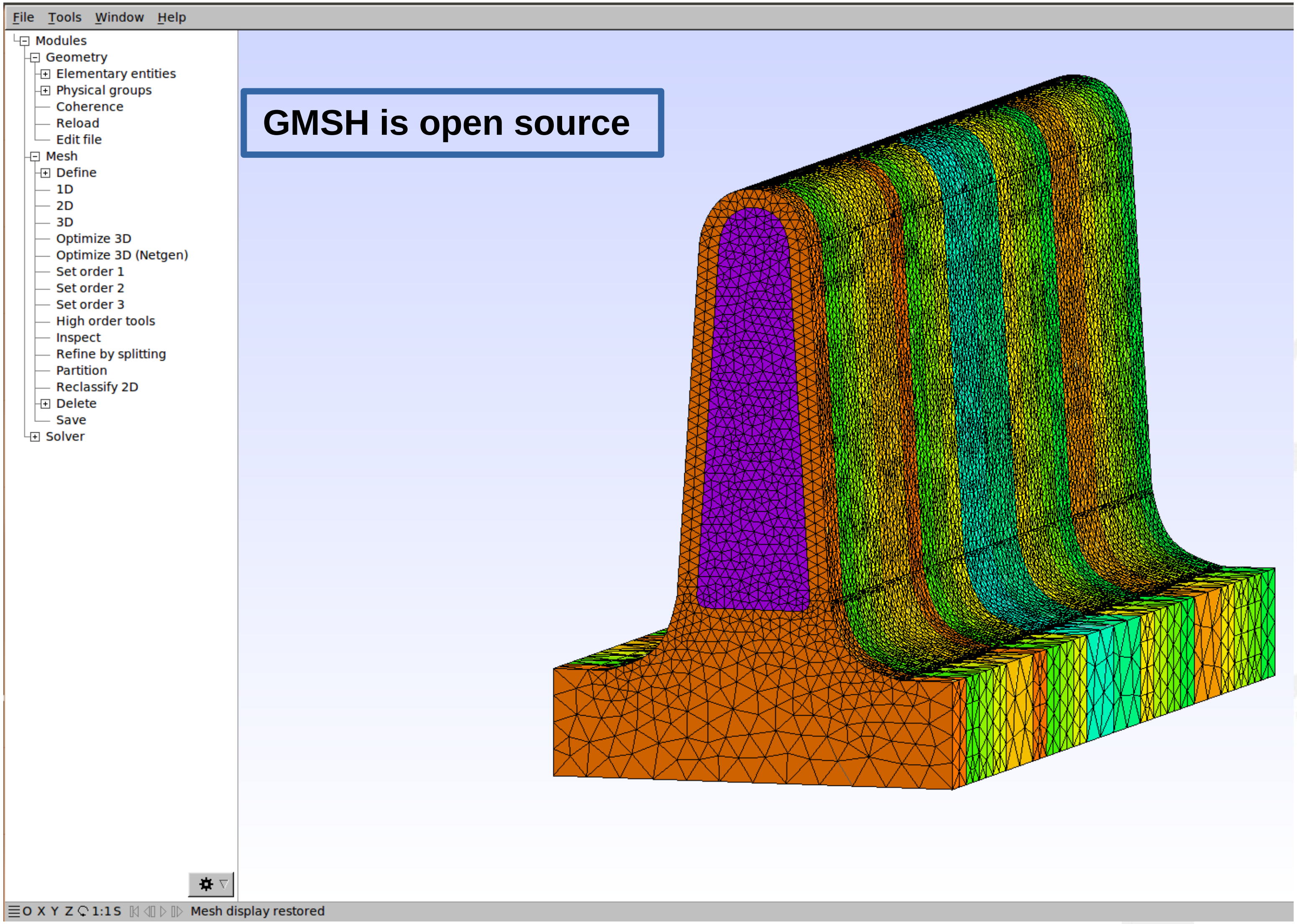

CiTIUS

GMSH: 3D finite element mesh generator
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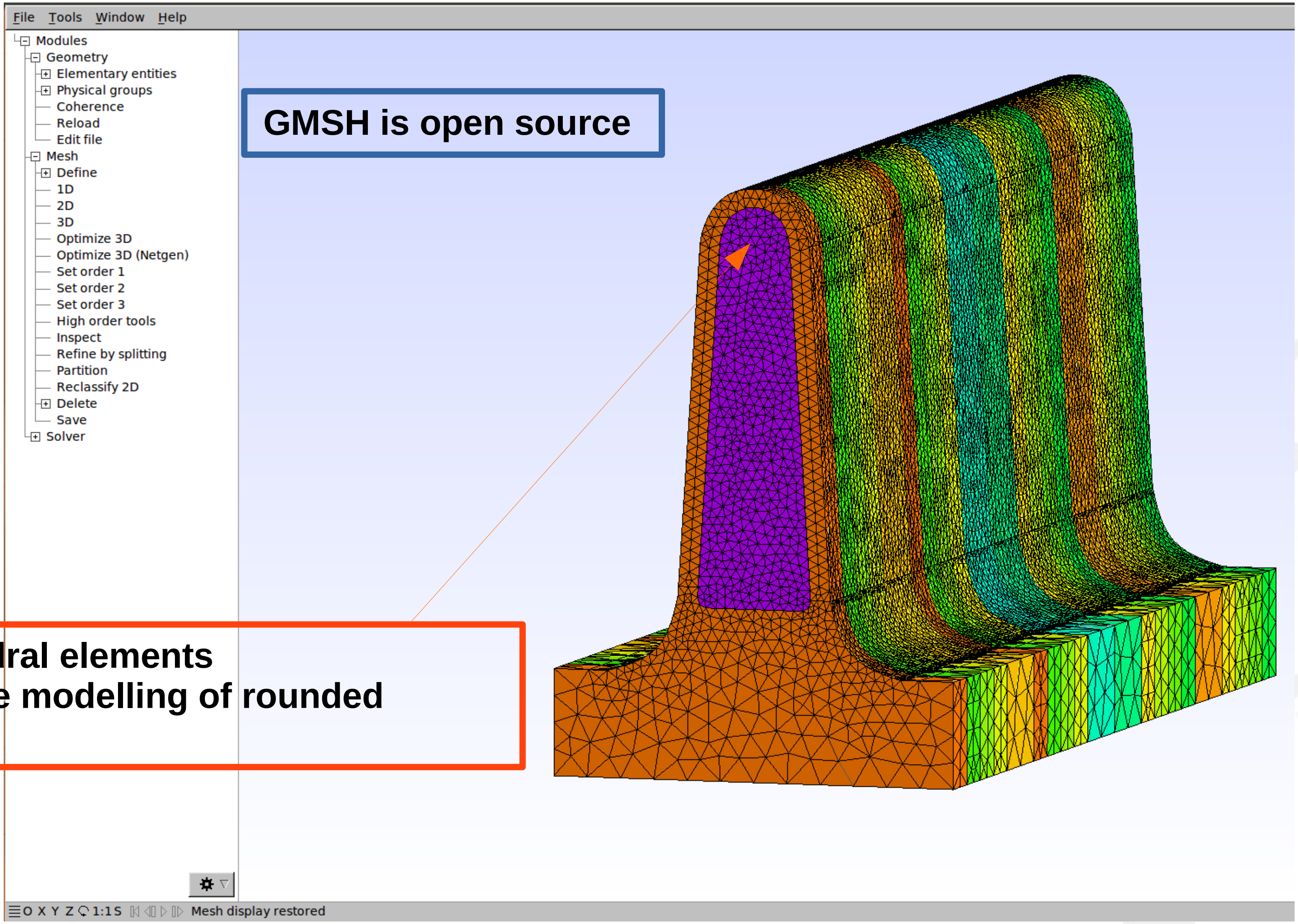
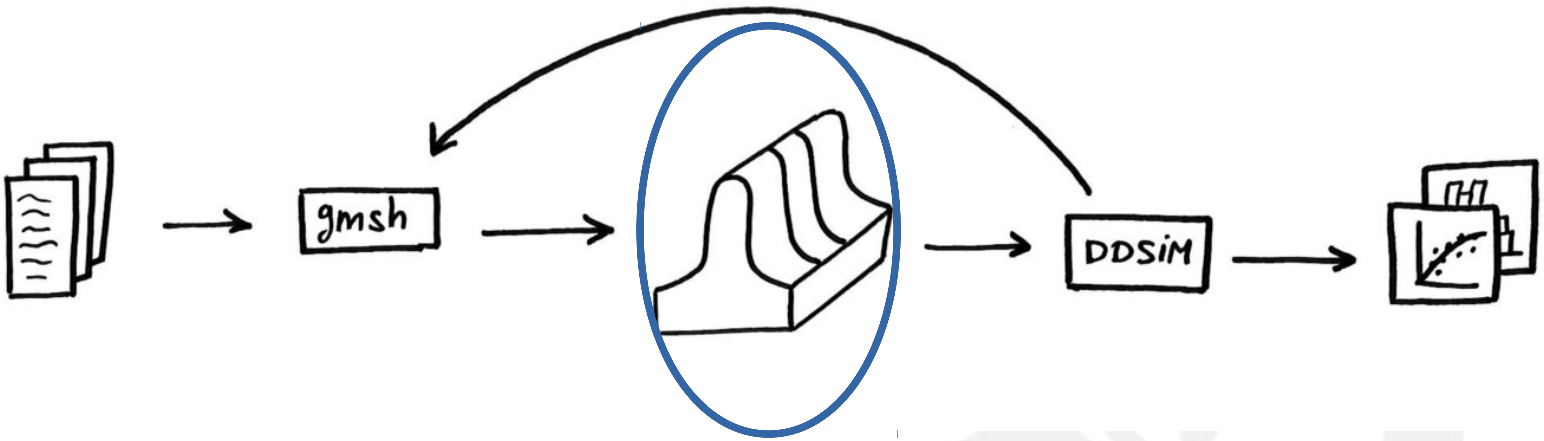


GMSH is open source

Tetrahedral elements
Accurate modelling of rounded corners

Simulation pipeline



Pre-processing stage

Pre-processing stage

- Asign properties to the mesh nodes (eg. Material, mobility, afinitity, permitivity..)
- Identify contacts of the device
- Divide the mesh into subdomains

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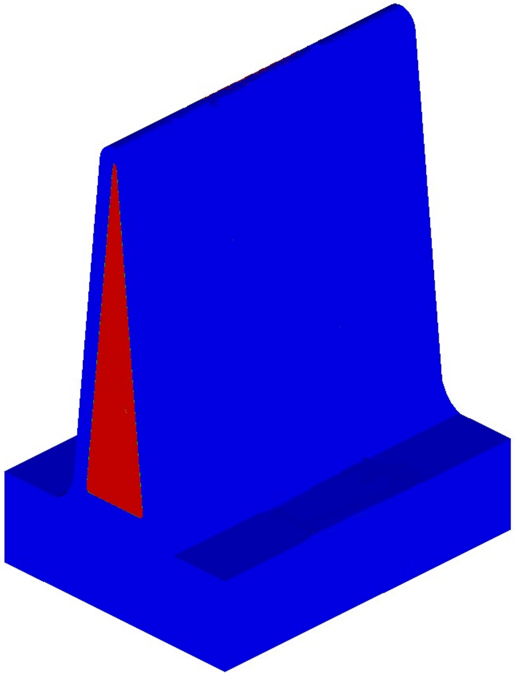

Triangular FinFET

Pre-processing stage

- Asign properties to the mesh nodes (eg. Material, mobility, afinitity, permitivity...)
- Identify contacts of the device
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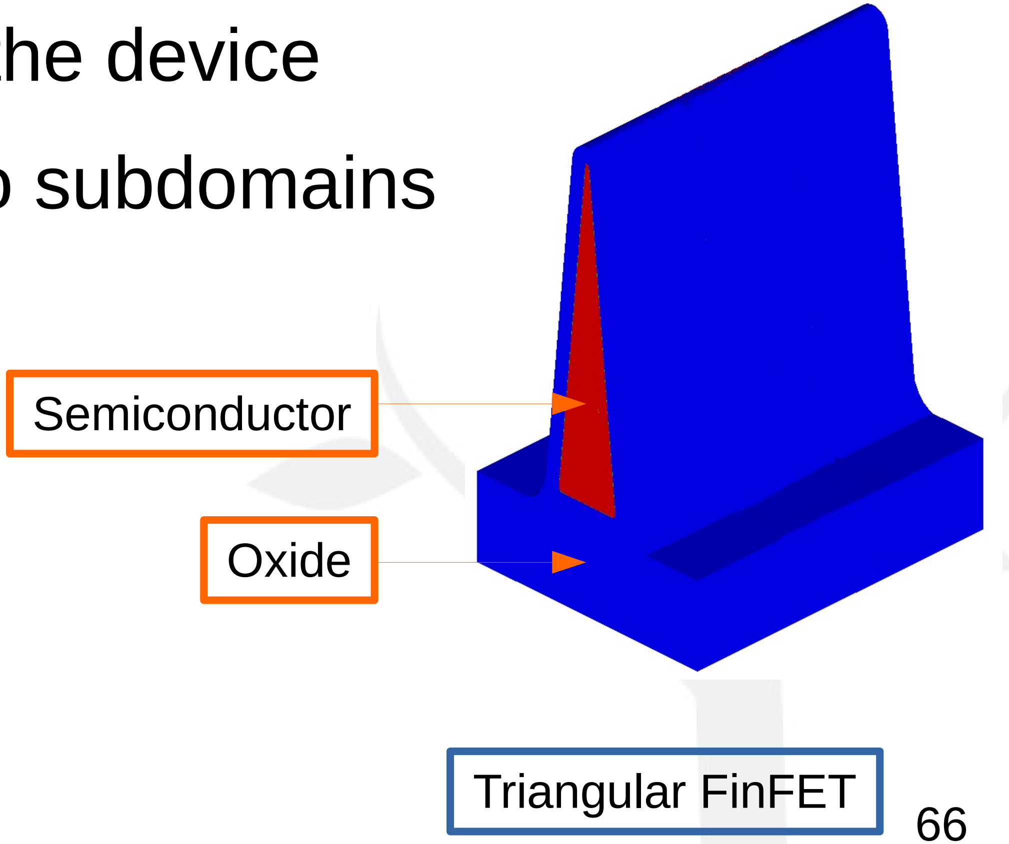

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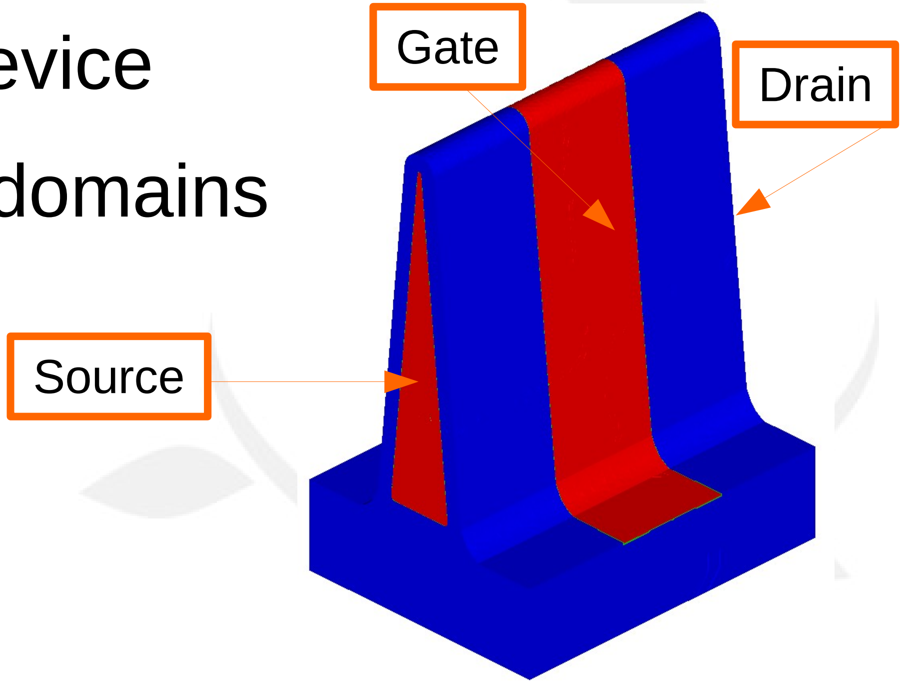

Triangular FinFET

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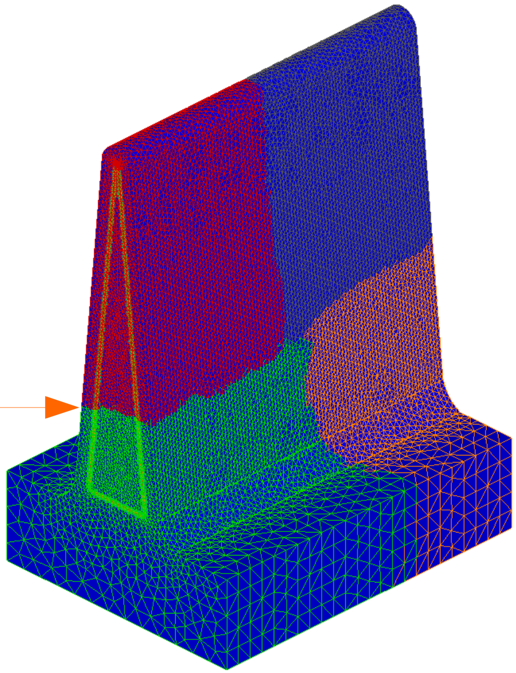
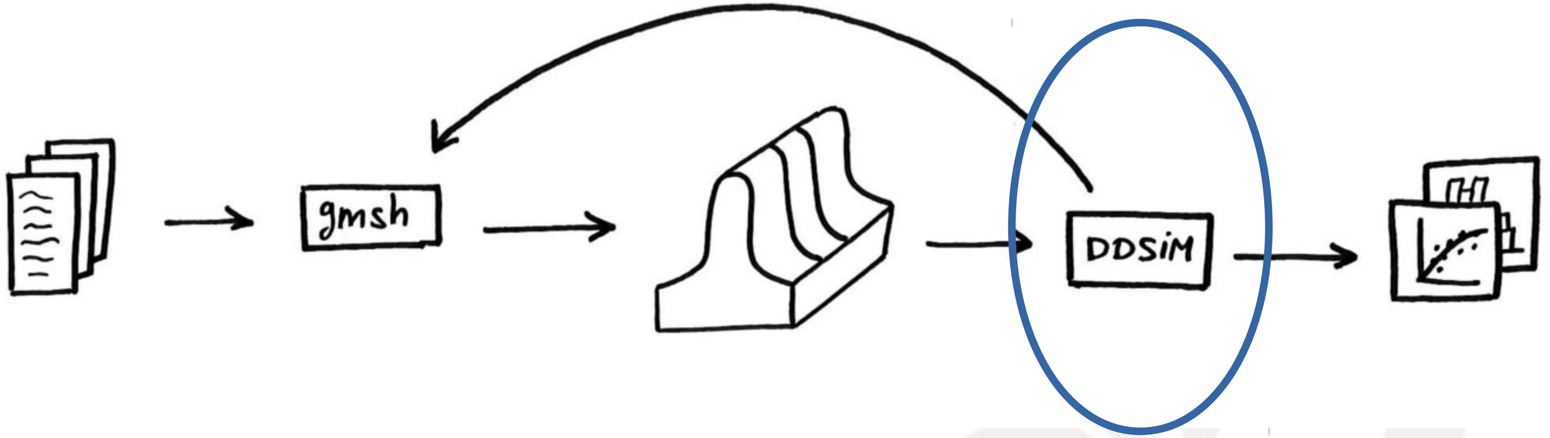


Simulation pipeline

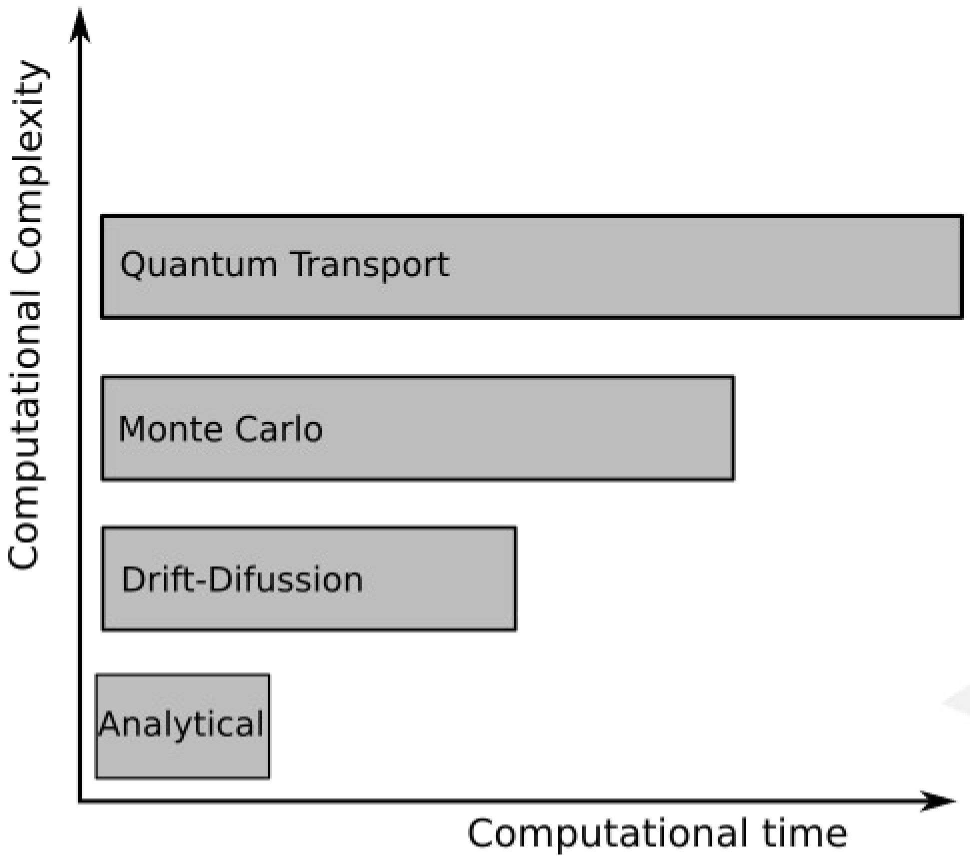


Simulation of the device

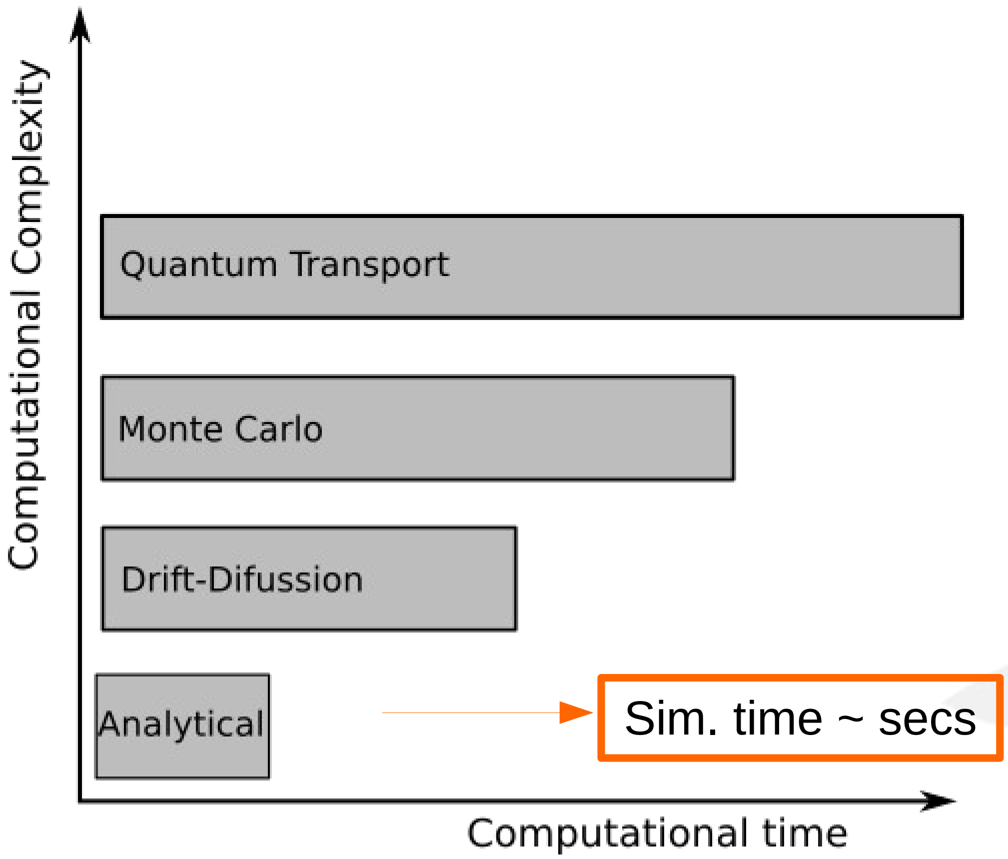
Simulation of the device

1. What is the **correct simulation method** for the device?
2. What are the main **limitations** of the chosen **model**?
3. What **kind of study** we want to perform?

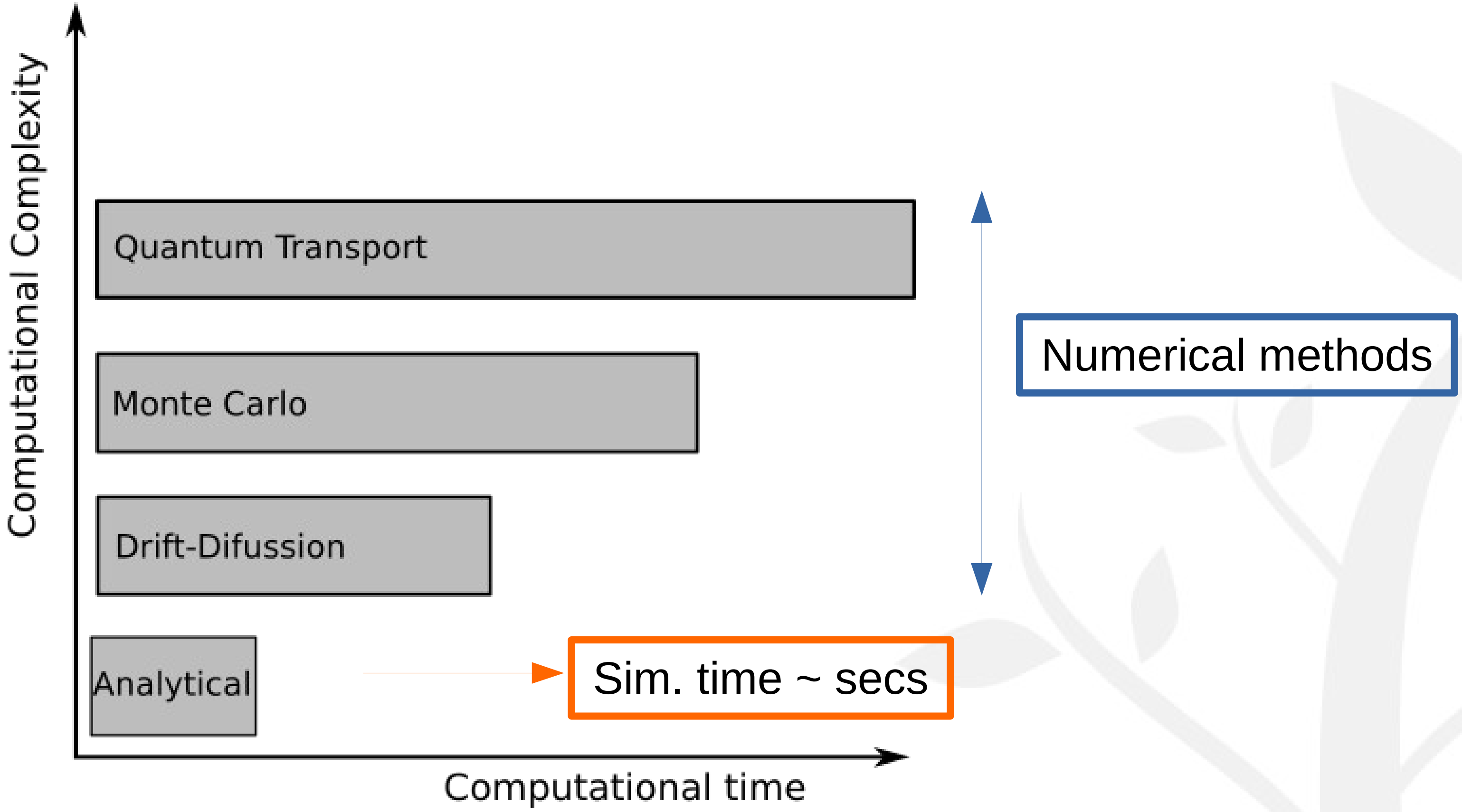
Simulation of the device



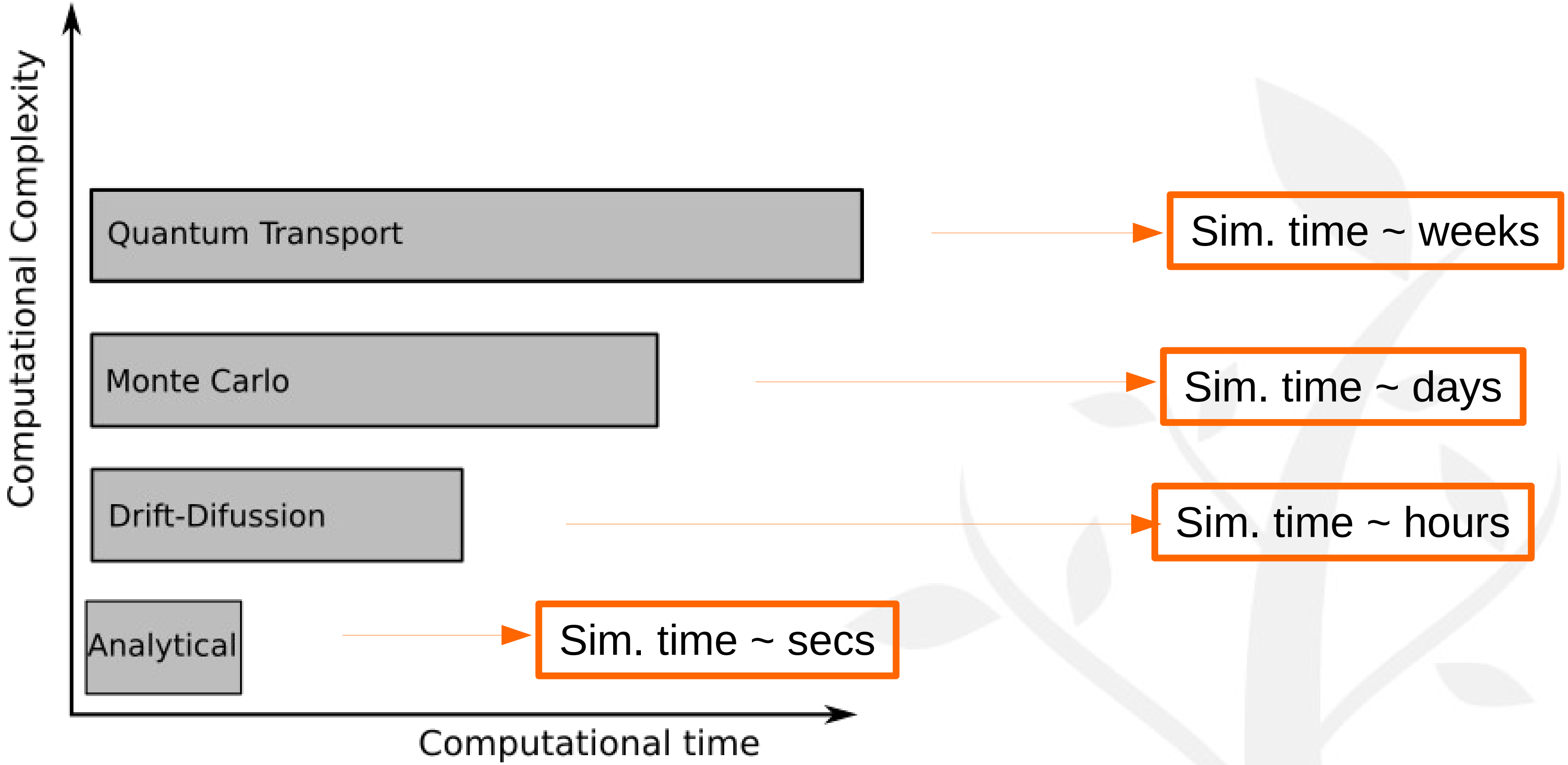
Simulation of the device



Simulation of the device



Simulation of the device



Simulation of the device

Example: Drift-difussion method

$$div(\varepsilon \nabla \phi) = q(p - n + N_D^+ - N_A^-)$$

$$2b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} = \phi_n - \phi + \frac{k_B T}{q} \ln\left(\frac{n}{n_i}\right)$$

$$2b_p \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} = \phi - \phi_p + \frac{k_B T}{q} \ln\left(\frac{p}{p_i}\right)$$

$$J_n = -q\mu_n n \nabla(\phi_n)$$

$$J_p = -q\mu_p p \nabla(\phi_p)$$

$$div(J_n) = qR$$

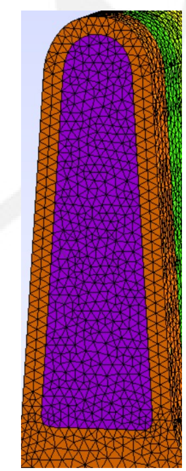
$$div(J_p) = -qR$$

Electrostatic potential

Current density

Electron concentration

Equations solved for each node of the mesh



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Limitations:

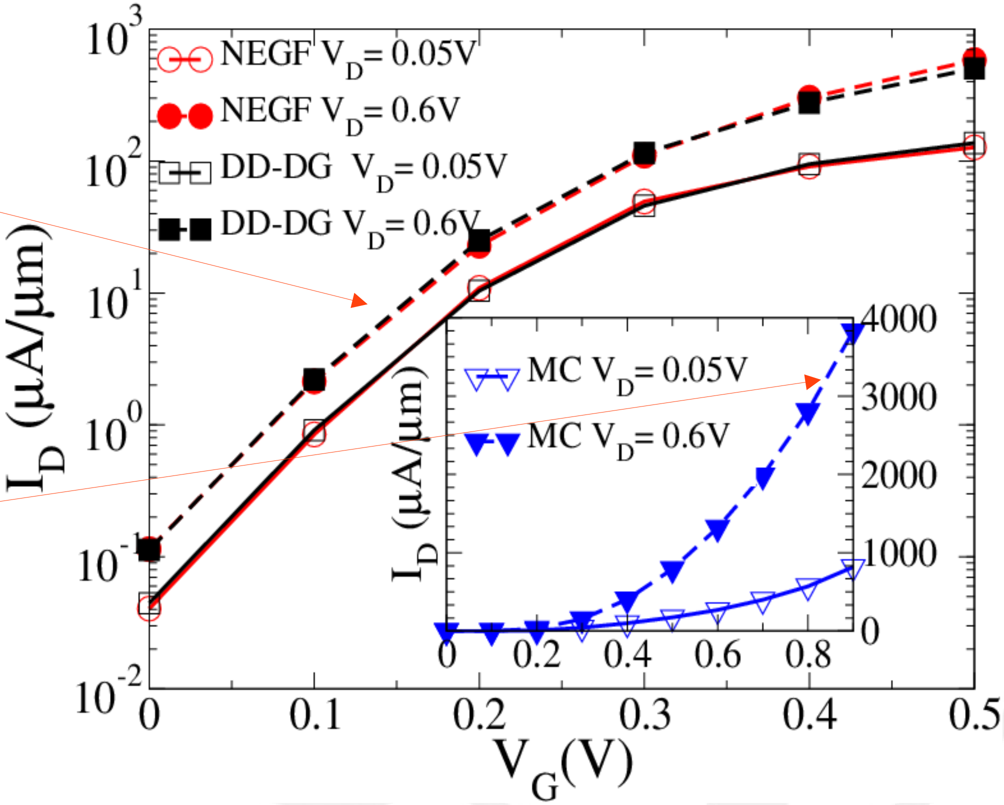
- Calibration required
  - Experimental data if available
  - More complex and accurate simulation methods
- Not valid for on-region studies

Calibration

10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFETs

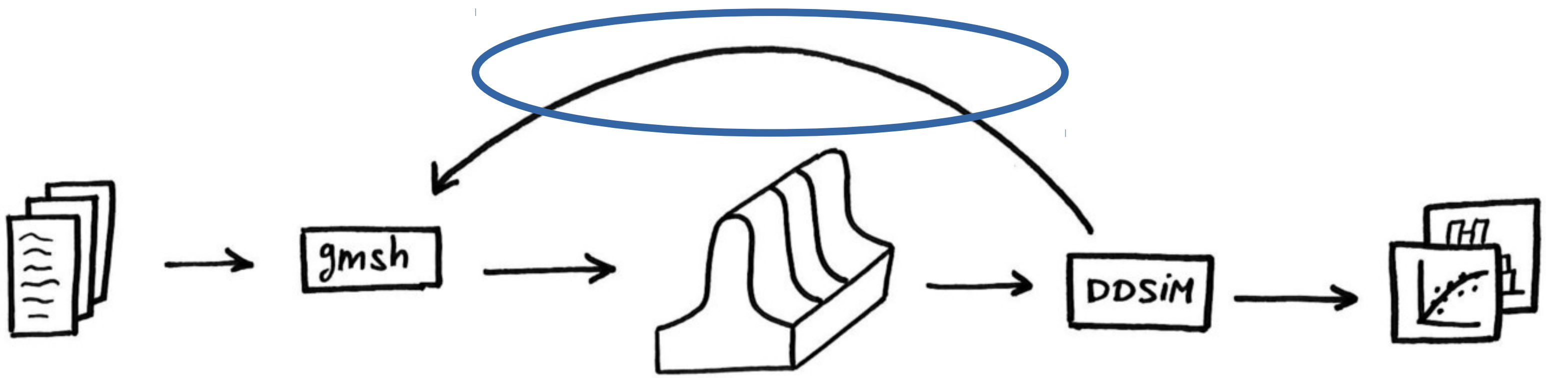
Drift-diffusion simulator used in the **sub-threshold region**: **calibrated** against NEGF simulations

Monte Carlo simulator used in the **on region**

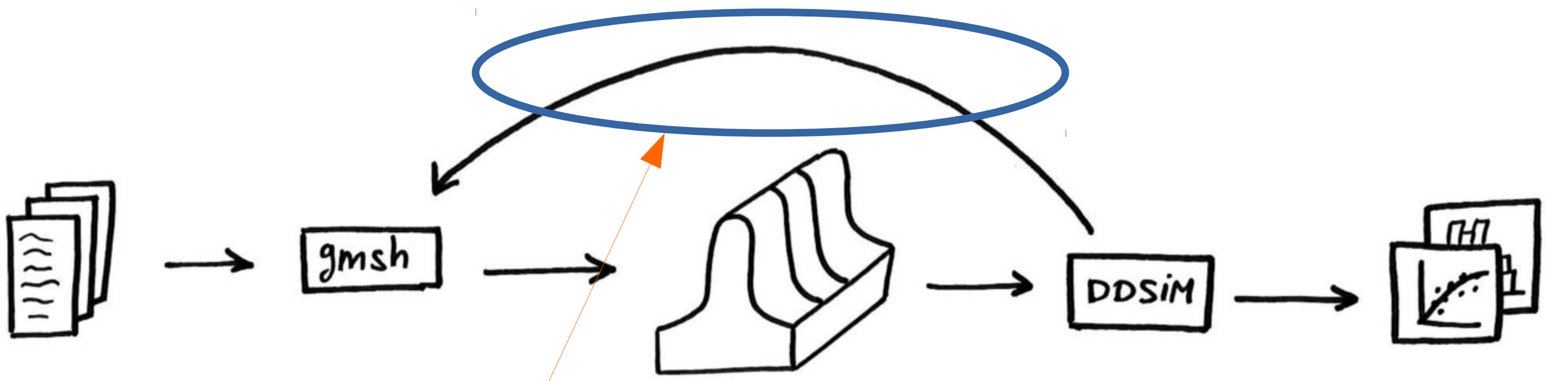


→ **Experimental data not available** yet

Simulation pipeline



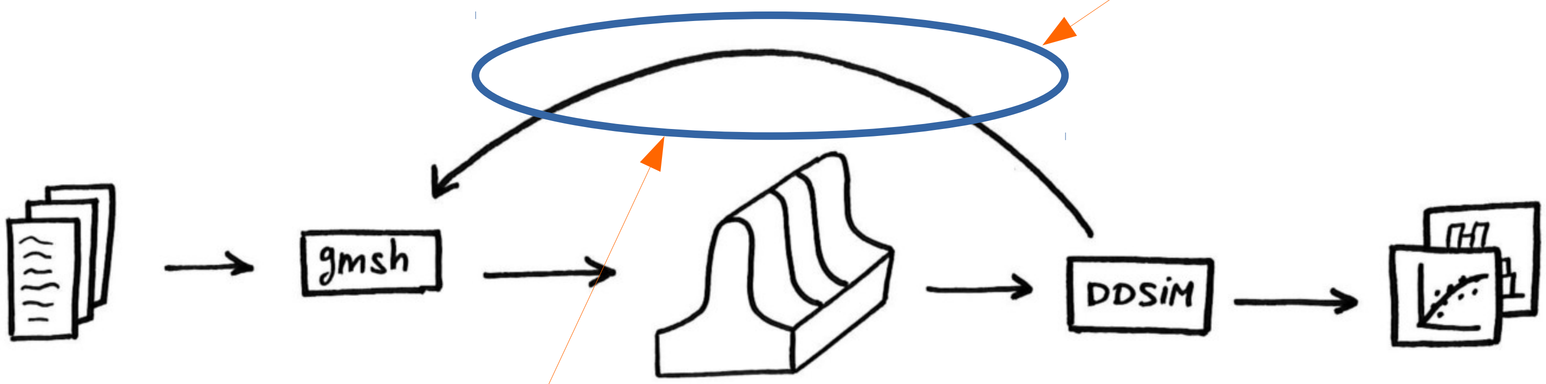
Simulation pipeline



Mesh too **coarse**: no convergence
Mesh too **fine**: increases the computational cost

Simulation pipeline

Selective refinement: special attention to transition areas and highly doped ones



Mesh too **coarse**: no convergence
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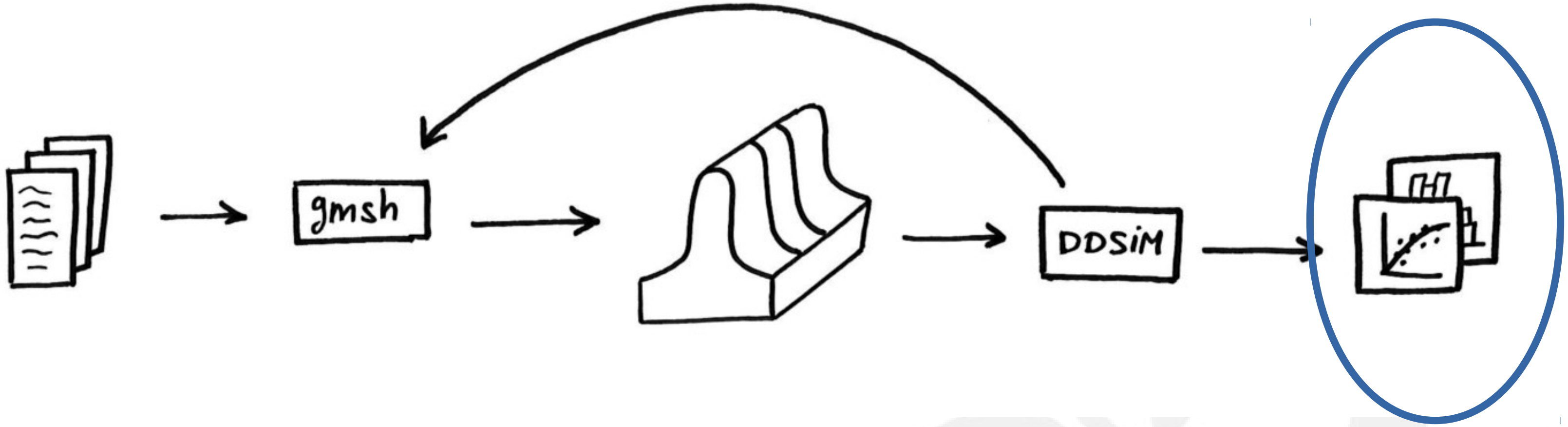
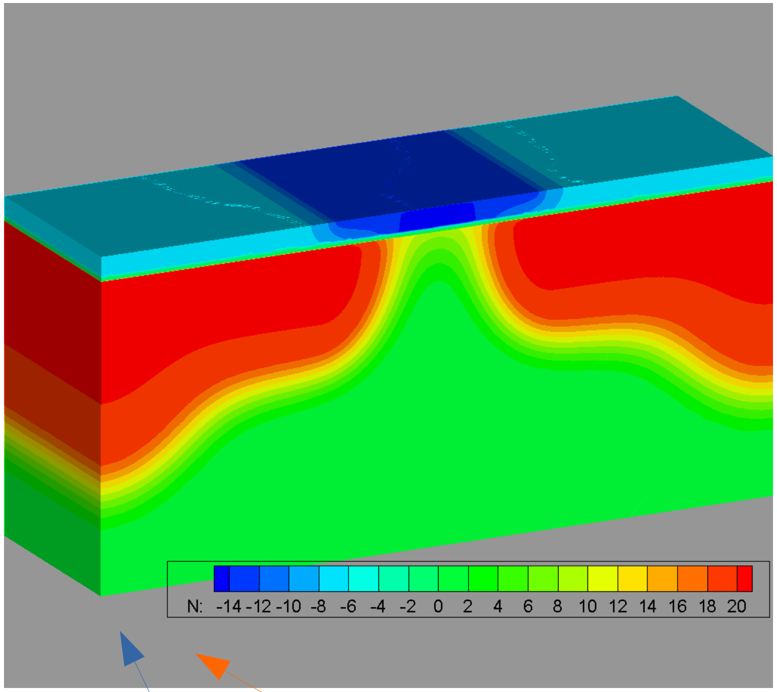
Simulation pipeline

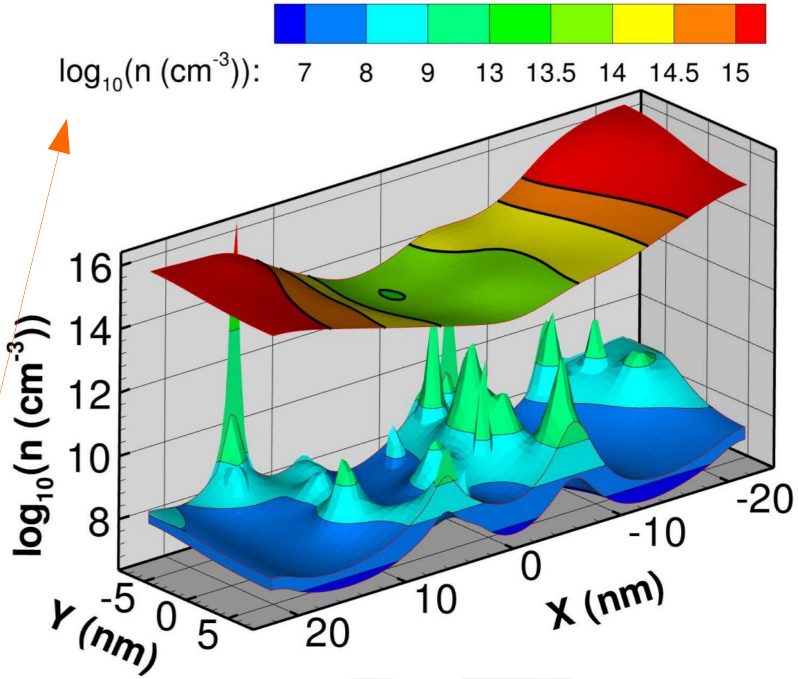


Analysis of the results

Analysis of the results

MOSFET devices

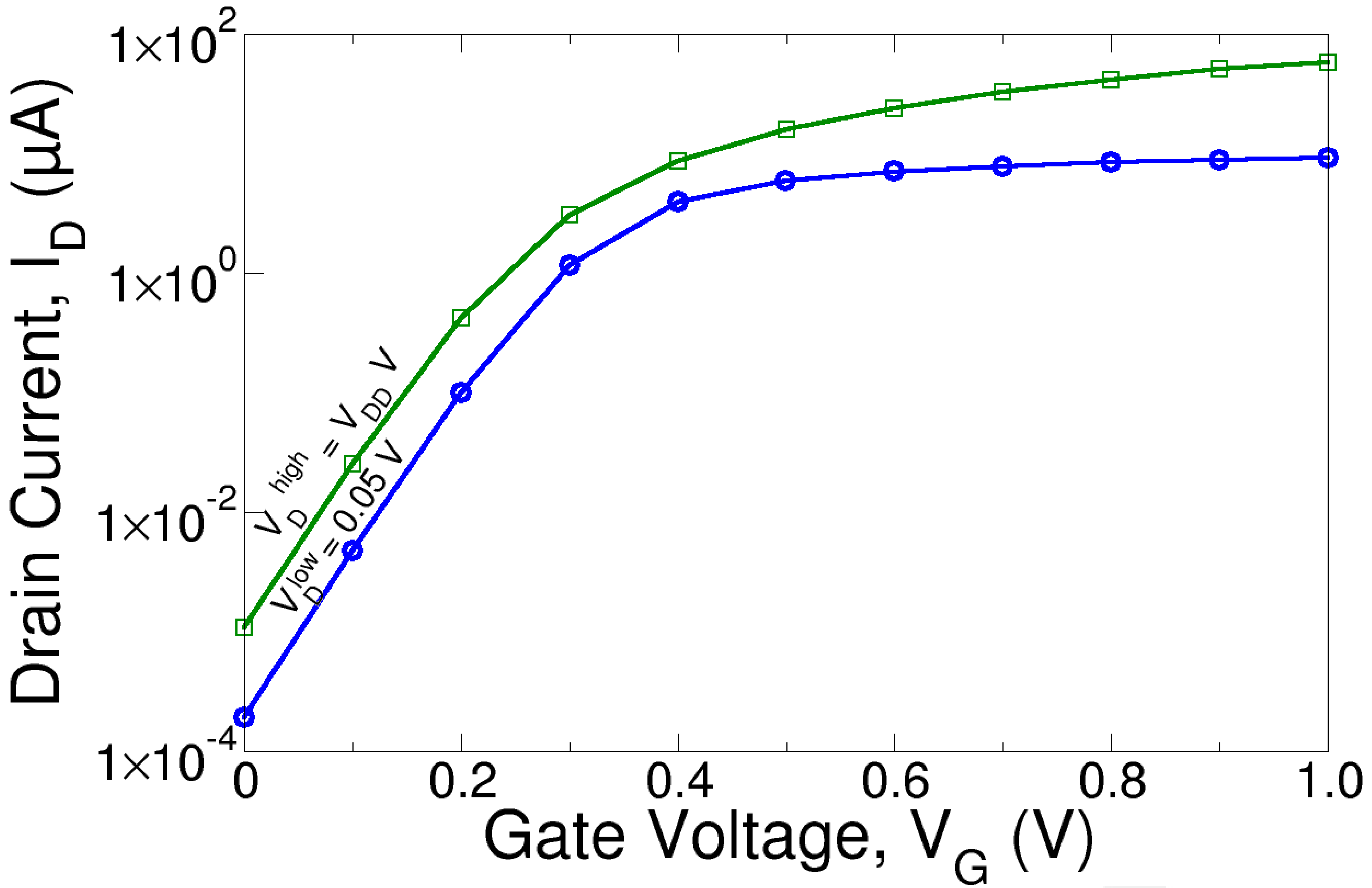




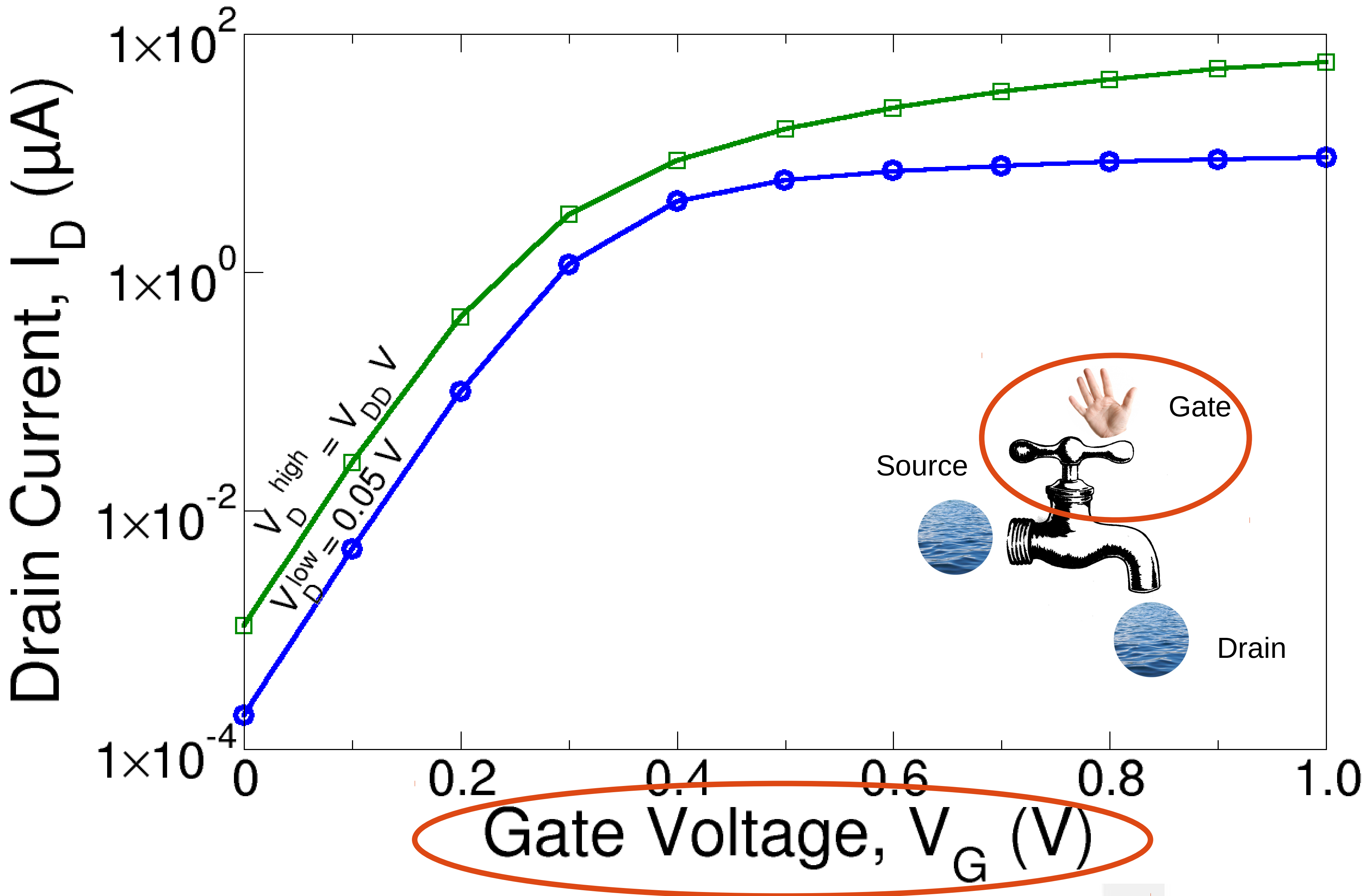
Electron concentration

Calculated at every point of the device

Analysis of the results



Analysis of the results



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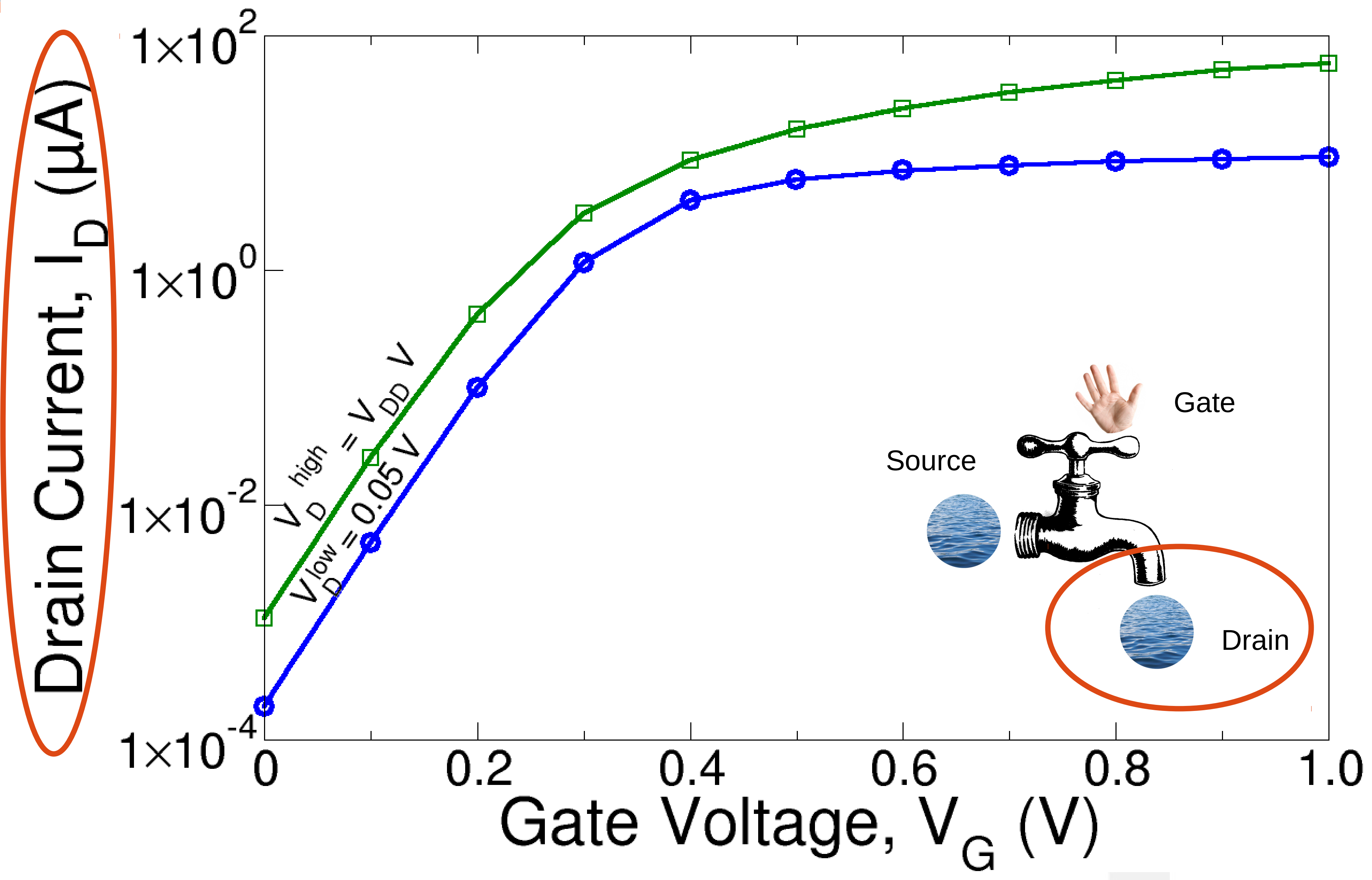

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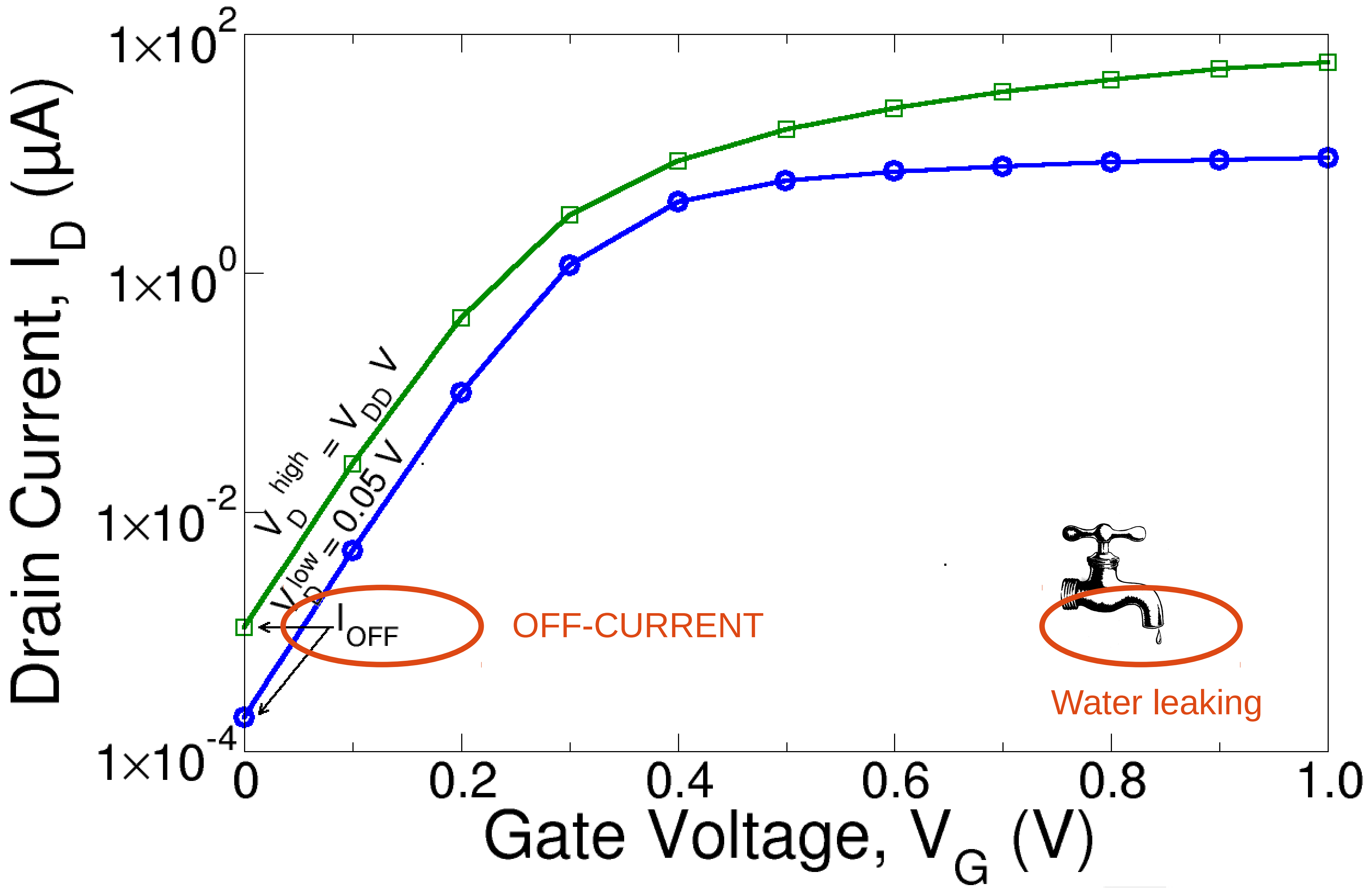

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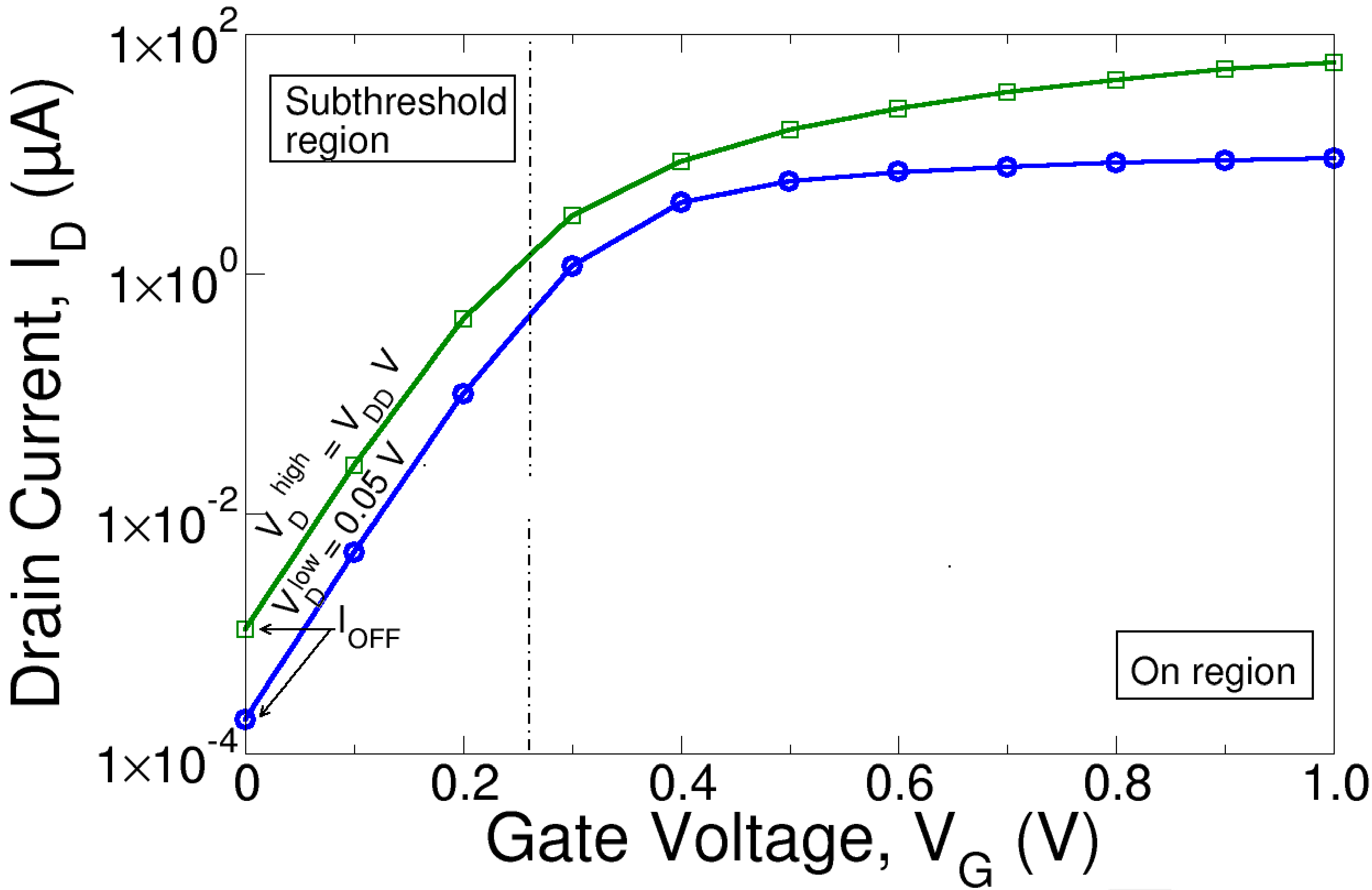
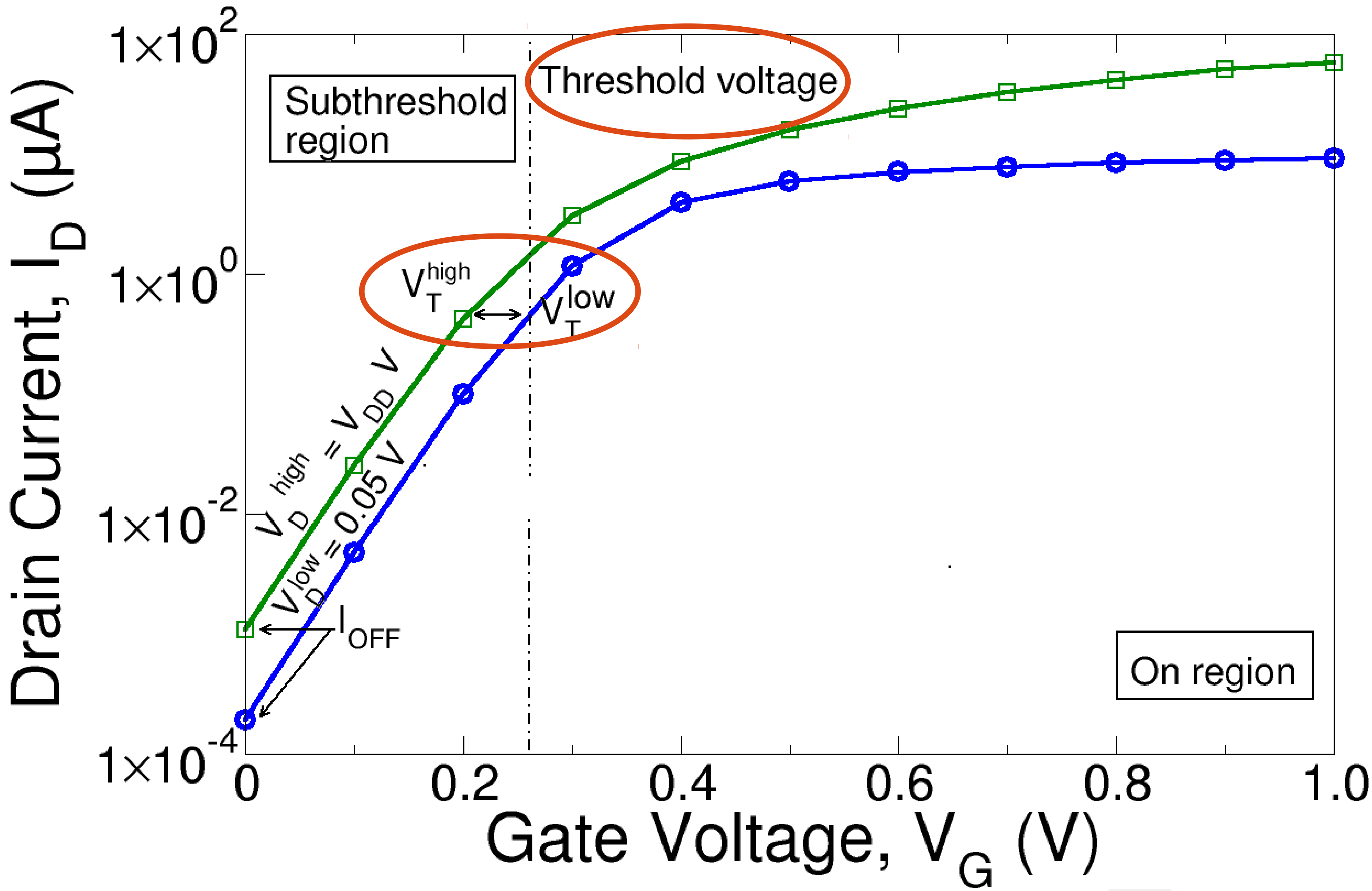
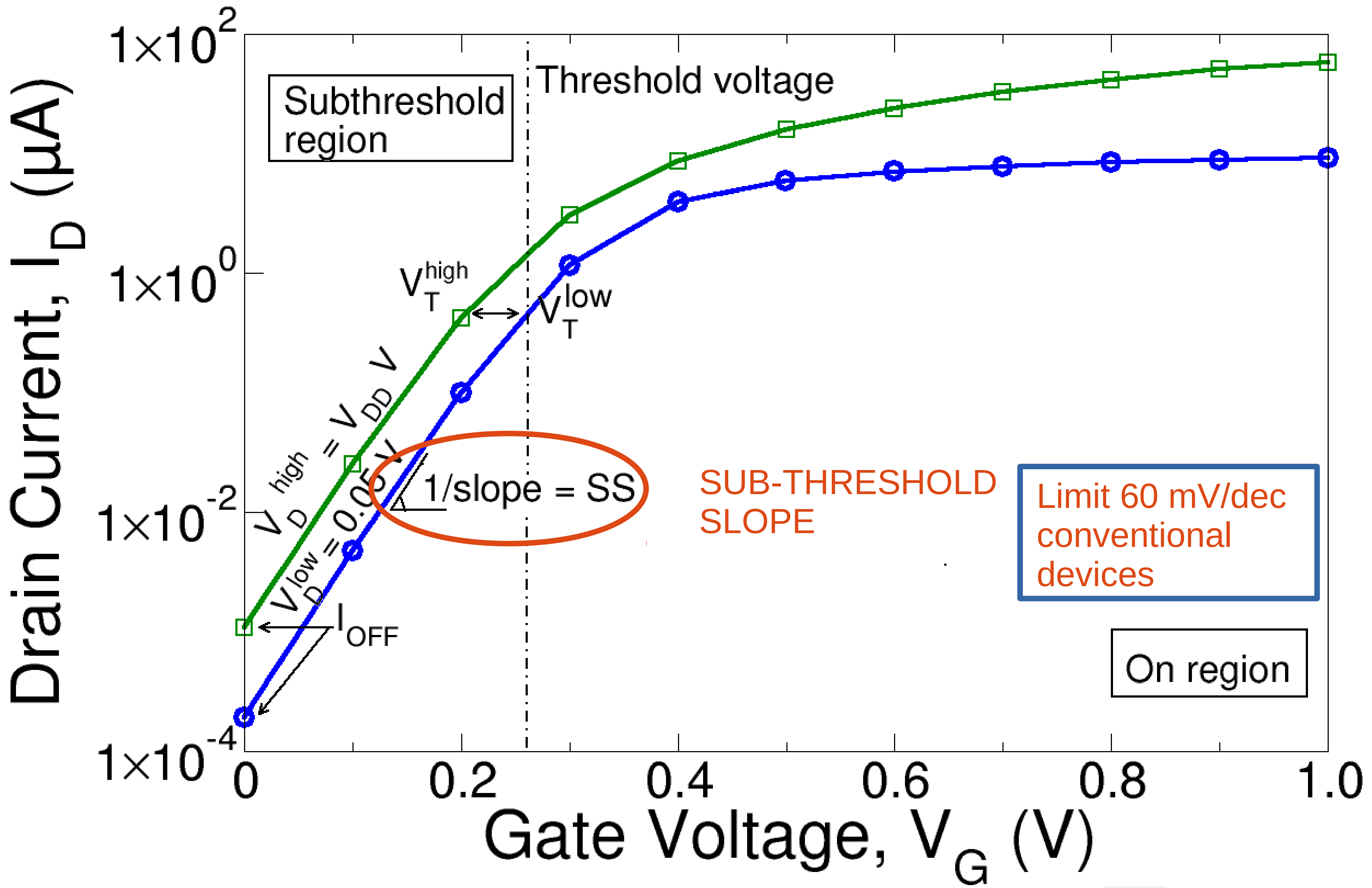


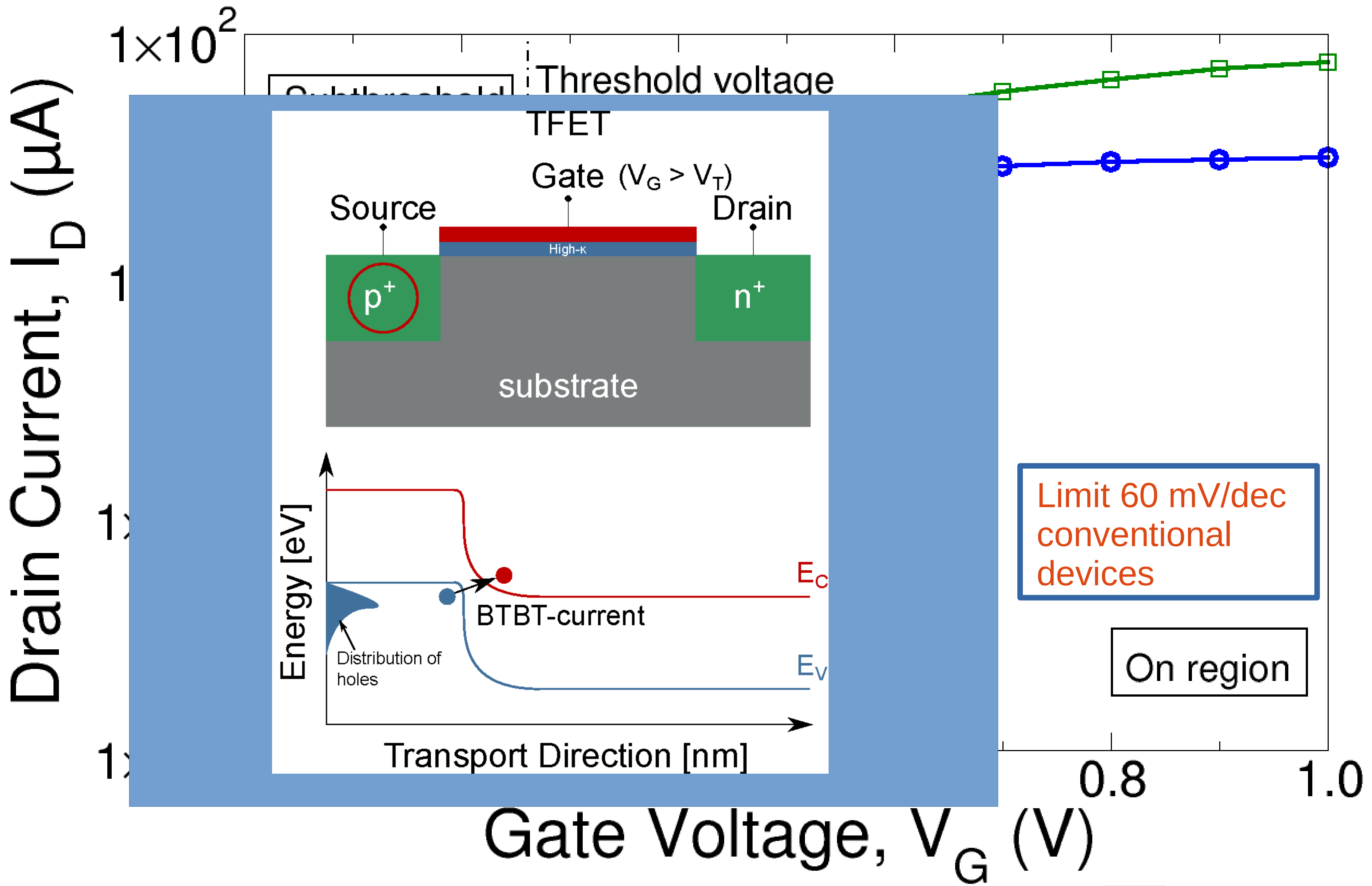
Analysis of the results



Analysis of the results



Analysis of the results



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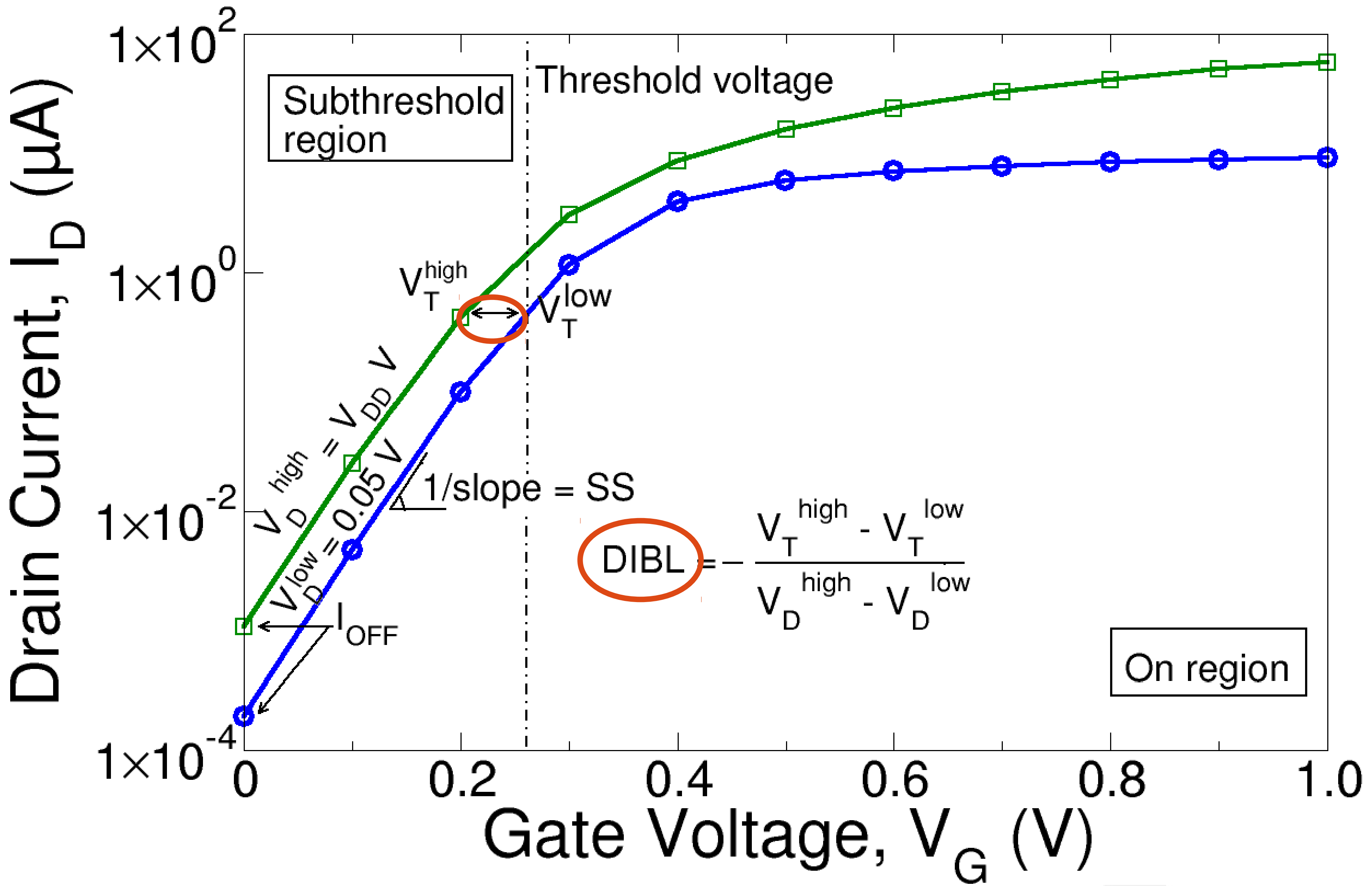

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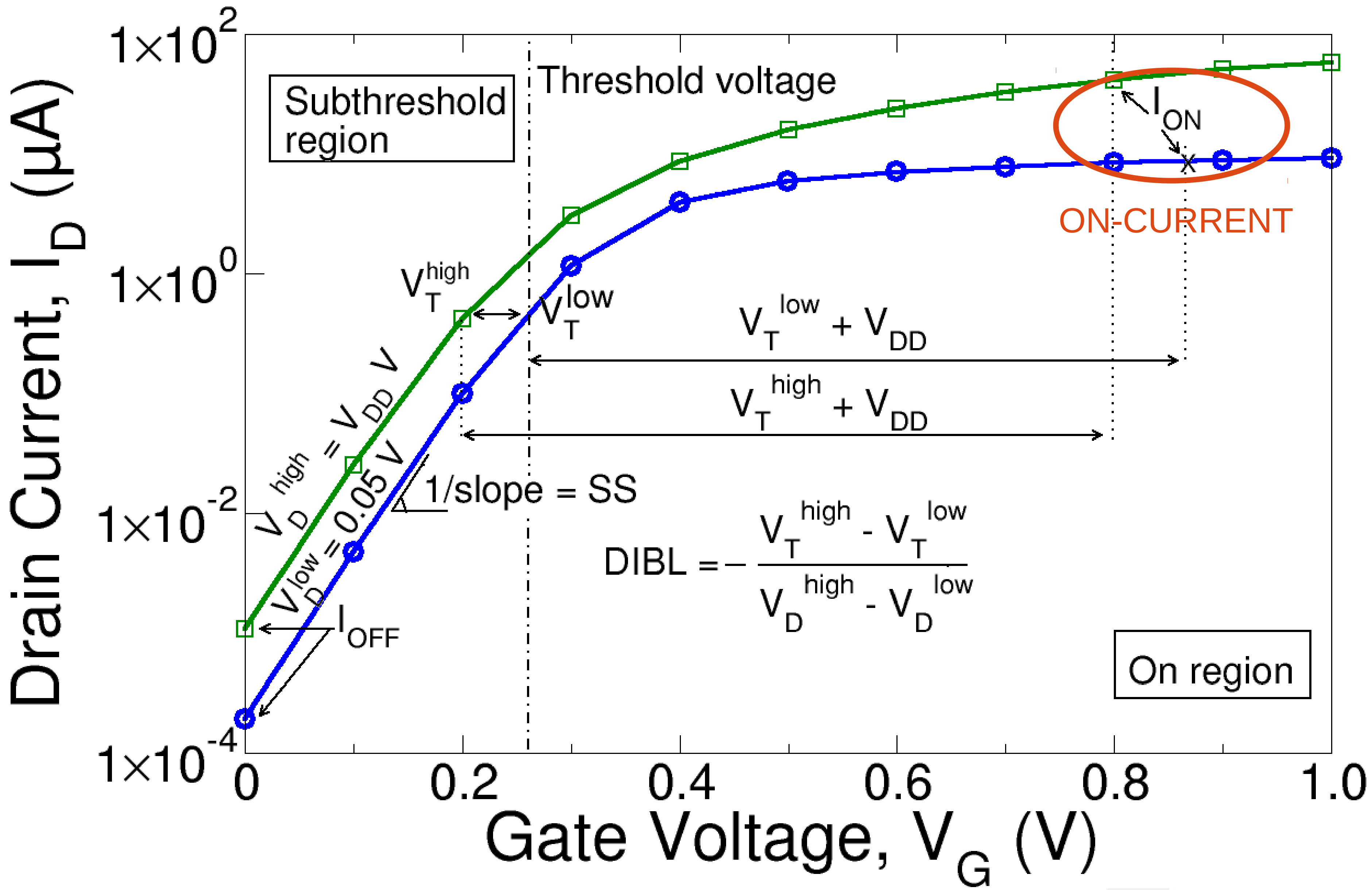

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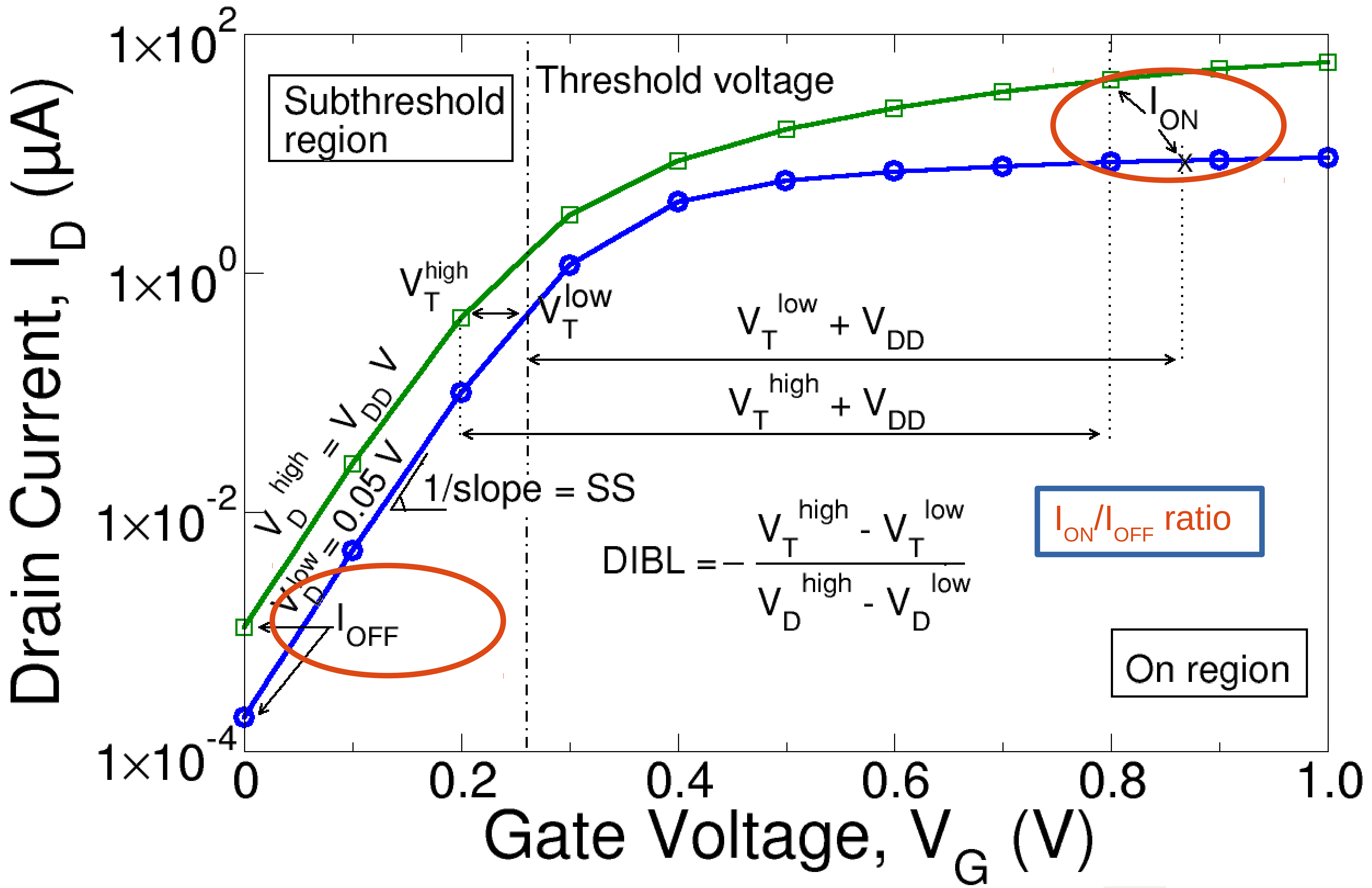


Outline

- Motivation
- Simulation methodology
- **Results**
- Conclusion

Results

- Why do we care about variability?
- Variability pipeline
- Variability sources
- How can we know more?

Why do we care about variability?

Example in the natural world

Picture a ladybird

Why do we care about variability?

Example in the natural world

Picture a ladybird

Or a **ladybug** if you think in American English

Why do we care about variability?

Example in the natural world

Picture a ladybird

Why do we care about variability?

Example in the natural world

Picture a ladybird

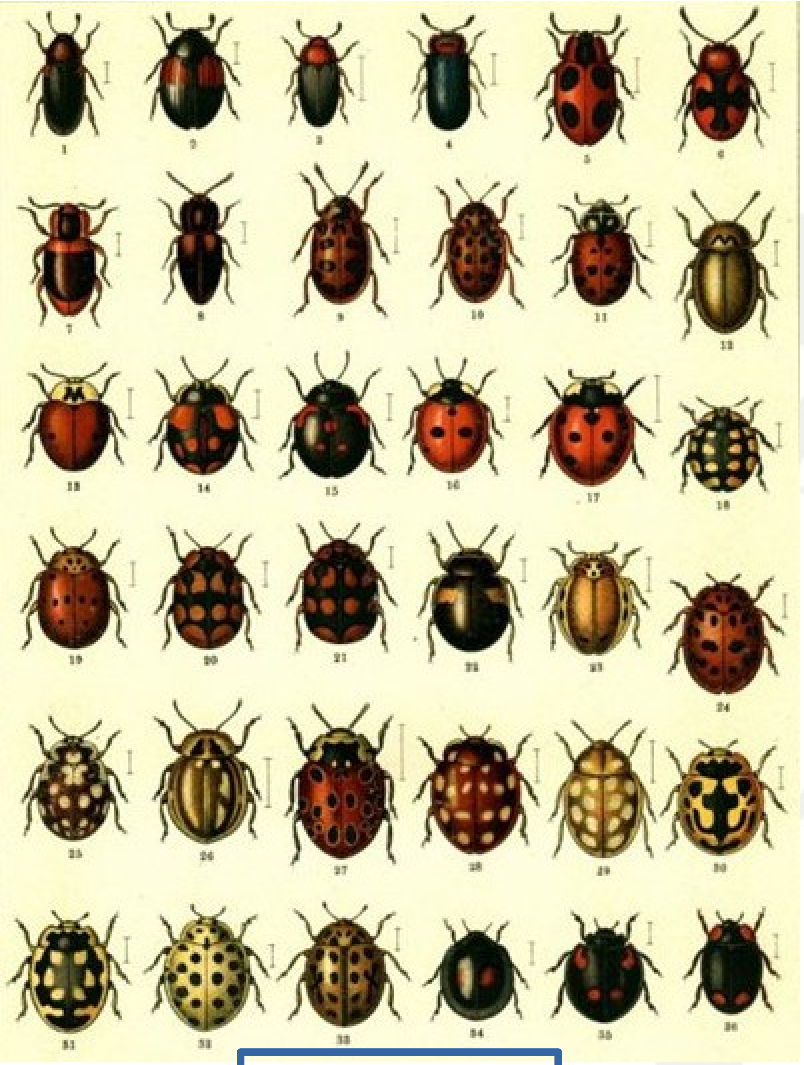
IDEAL

Why do we care about variability?

Example in the natural world

Picture a ladybird

IDEAL

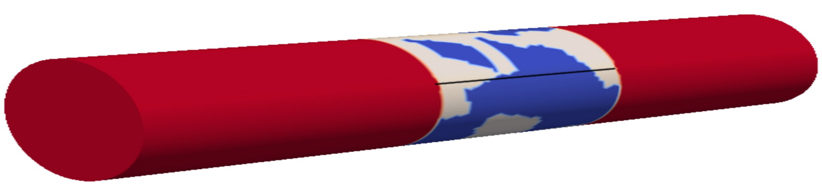


REALITY

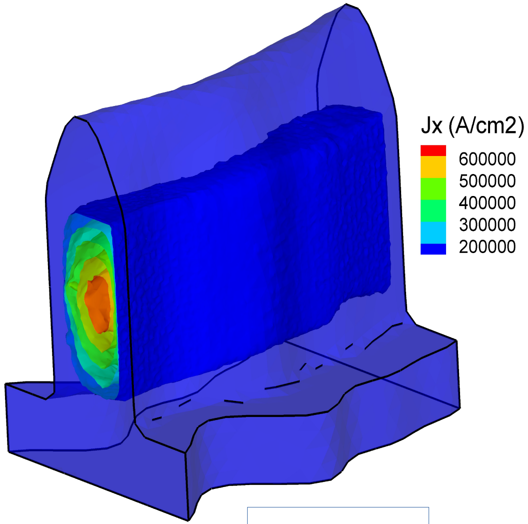
Why do we care about variability?

Importance

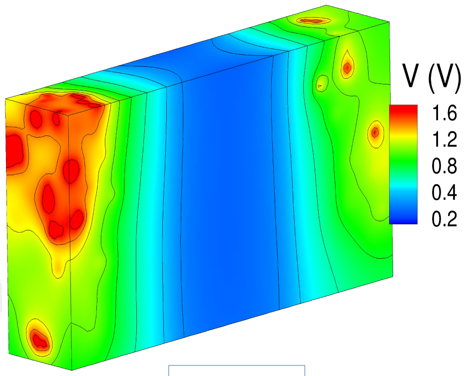
- **Variability sources** appear during **transistor fabrication** and have a **negative impact** on the final device **performance** and **reliability (chip failure)**
- This effect is becoming **more pronounced** for the state-of-the-art devices
- The **effect** of intrinsic sources of variability is **inherent** to the devices and **cannot be eliminated**



MGG



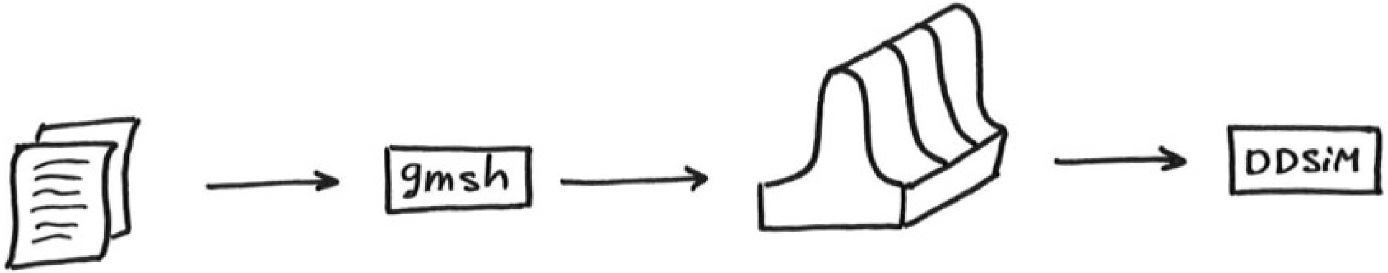
LER



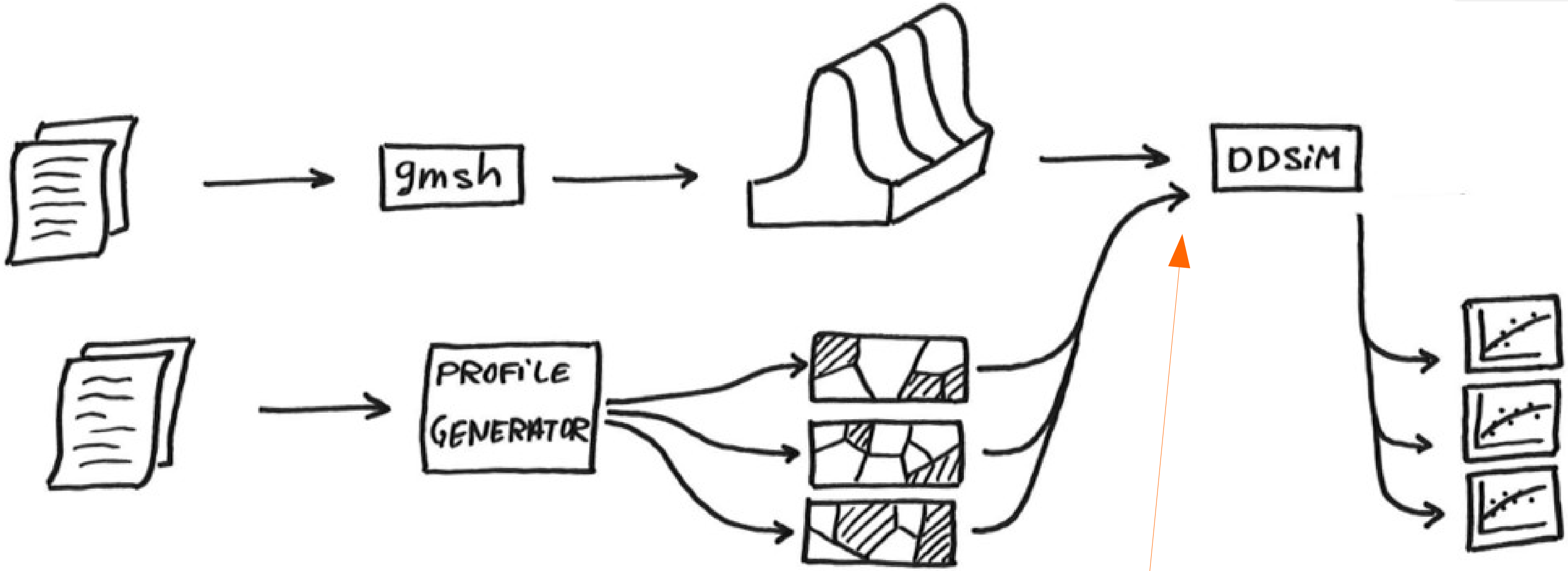
RD

Variability pipeline

We have simulated the ideal device

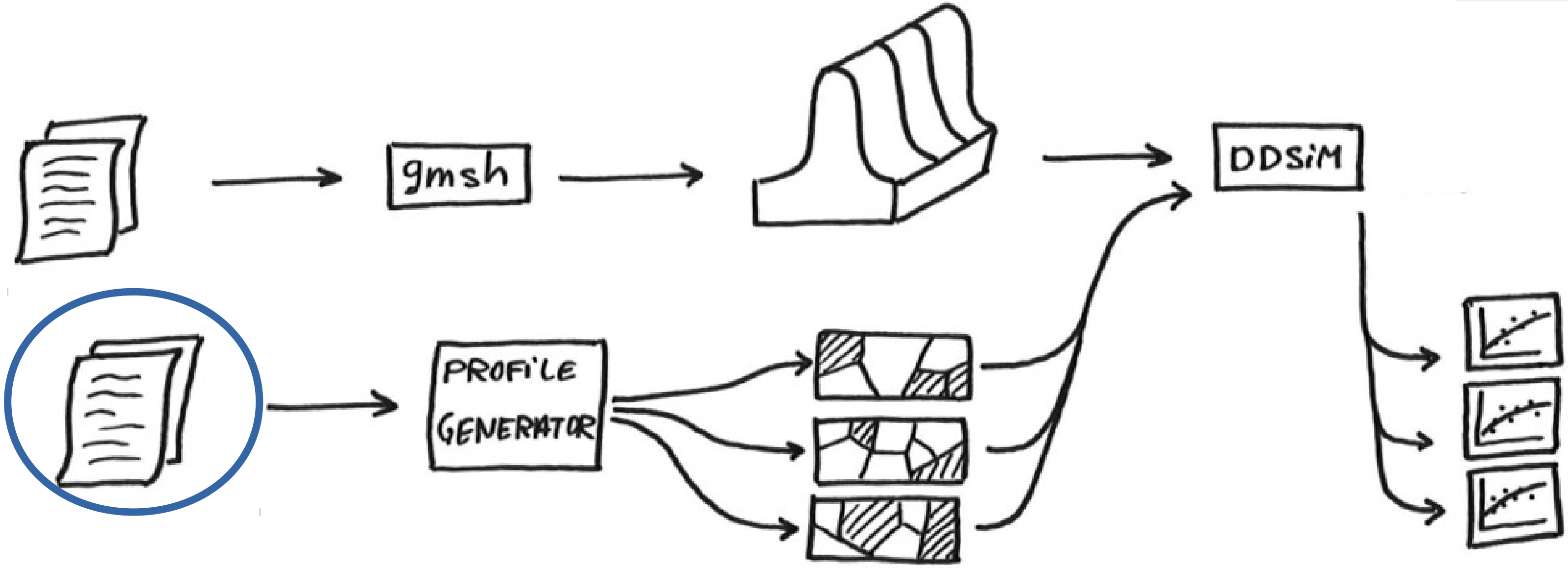


Variability pipeline



Variabililty introduced in the work-flow

Variability pipeline

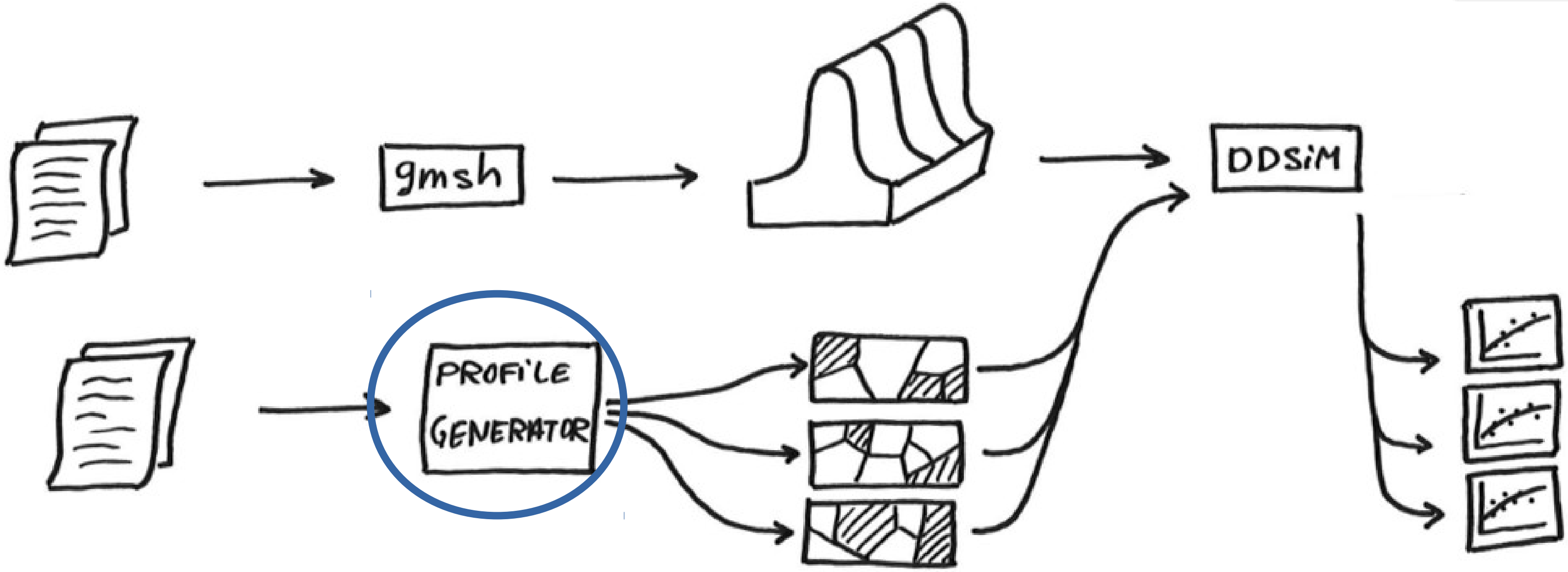


Data sources

Variabililty introduced in the work-flow

Variability pipeline

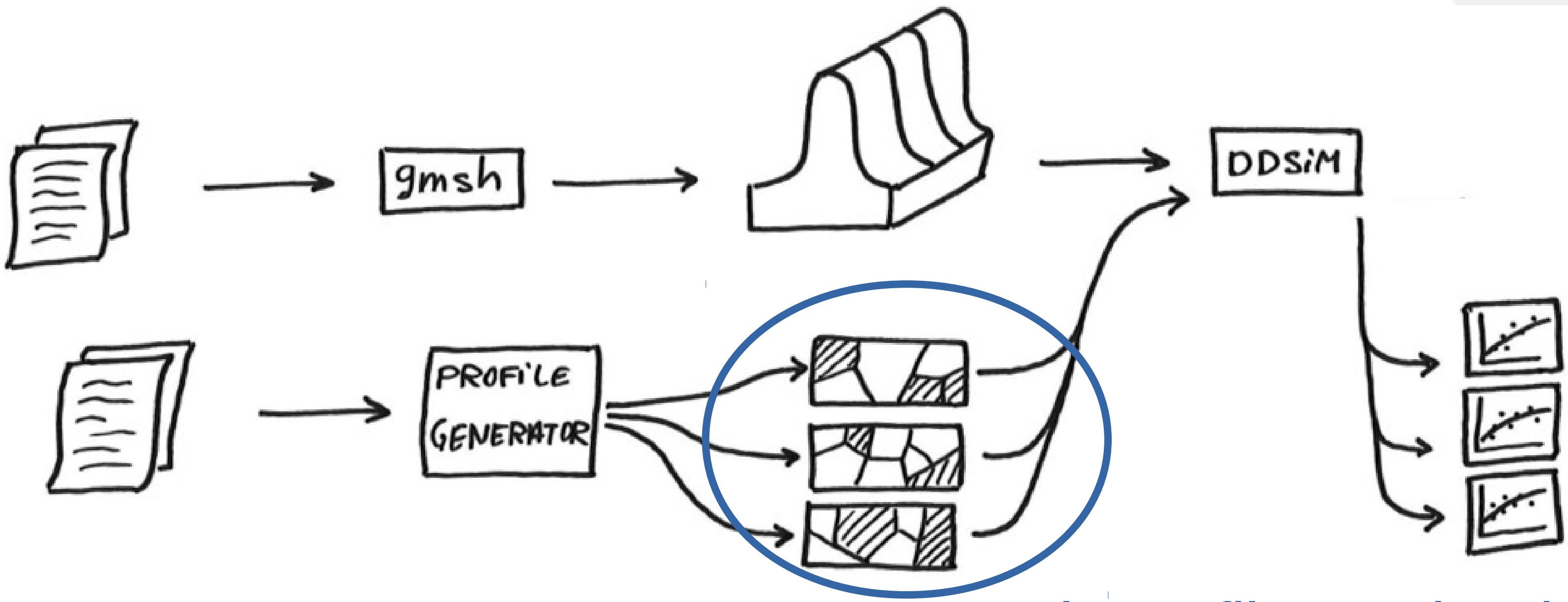
Profile: file that specifies the differences from the ideal device configuration



Generate profiles

Variabililty introduced in the work-flow

Variability pipeline

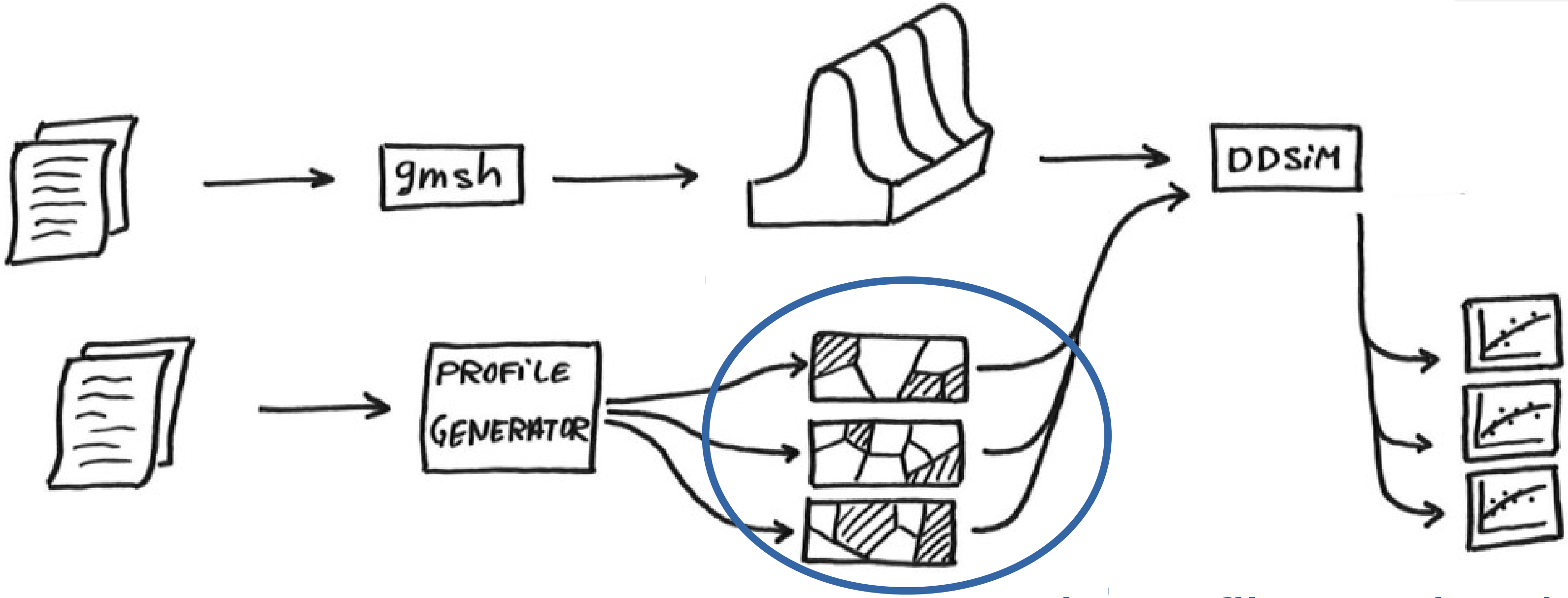


Apply profiles to the device

Variabililty introduced in the work-flow

Variability pipeline

Each profile → a new device needs to be simulated



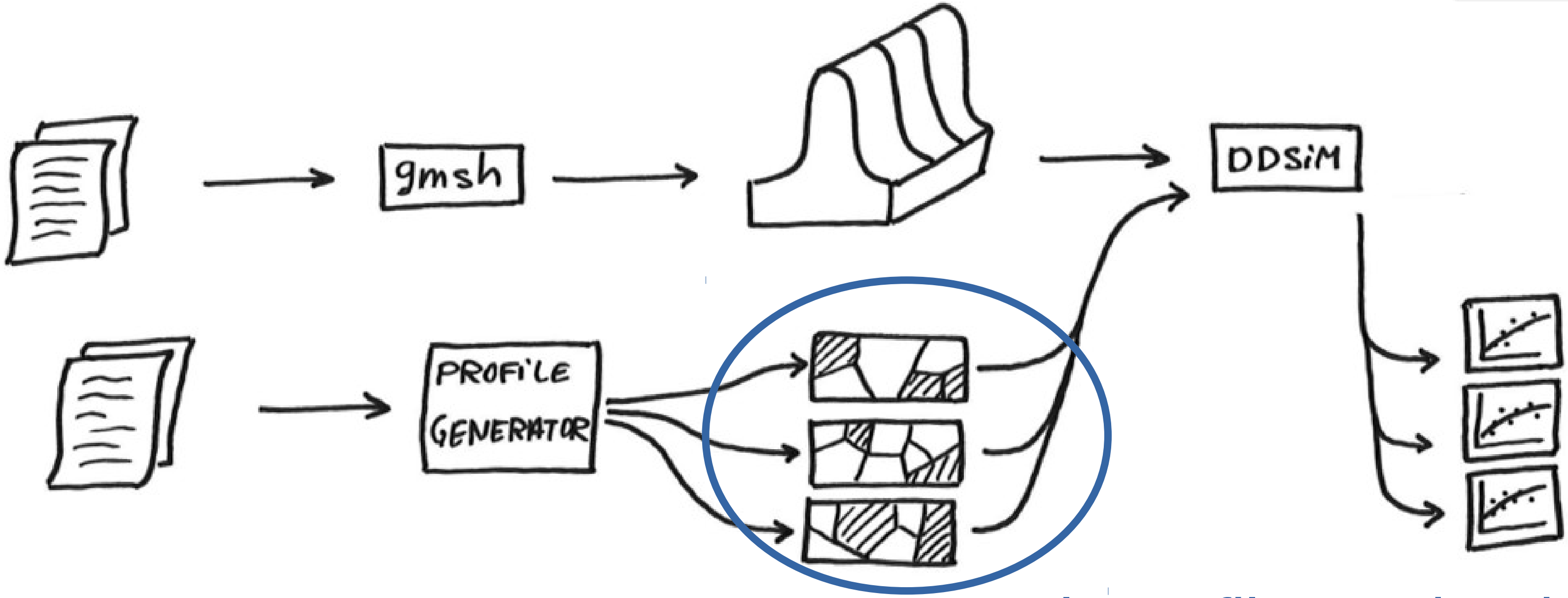
Apply profiles to the device

Variabililty introduced in the work-flow

Variability pipeline

Each profile → a new device needs to be simulated

Hundreds of devices



Apply profiles to the device

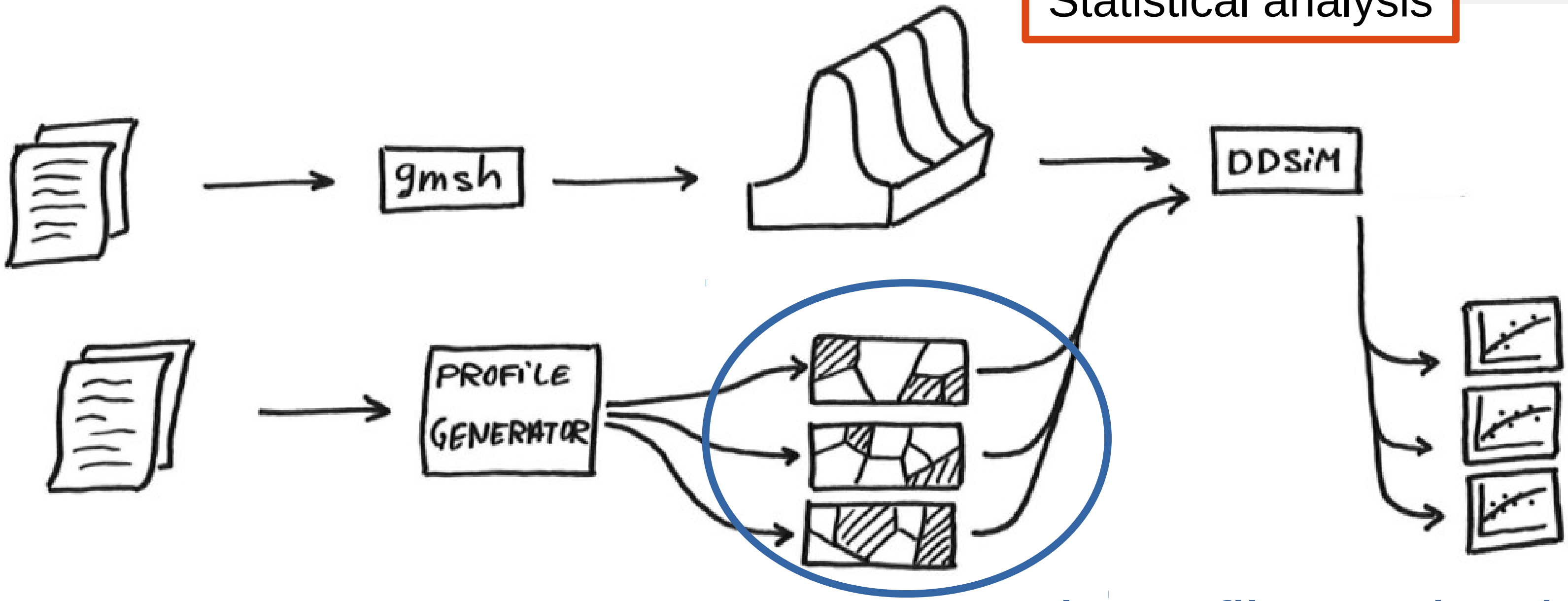
Variabililty introduced in the work-flow

Variability pipeline

Each profile → a new device needs to be simulated

Hundreds of devices

Statistical analysis



Apply profiles to the device

Variabililty introduced in the work-flow

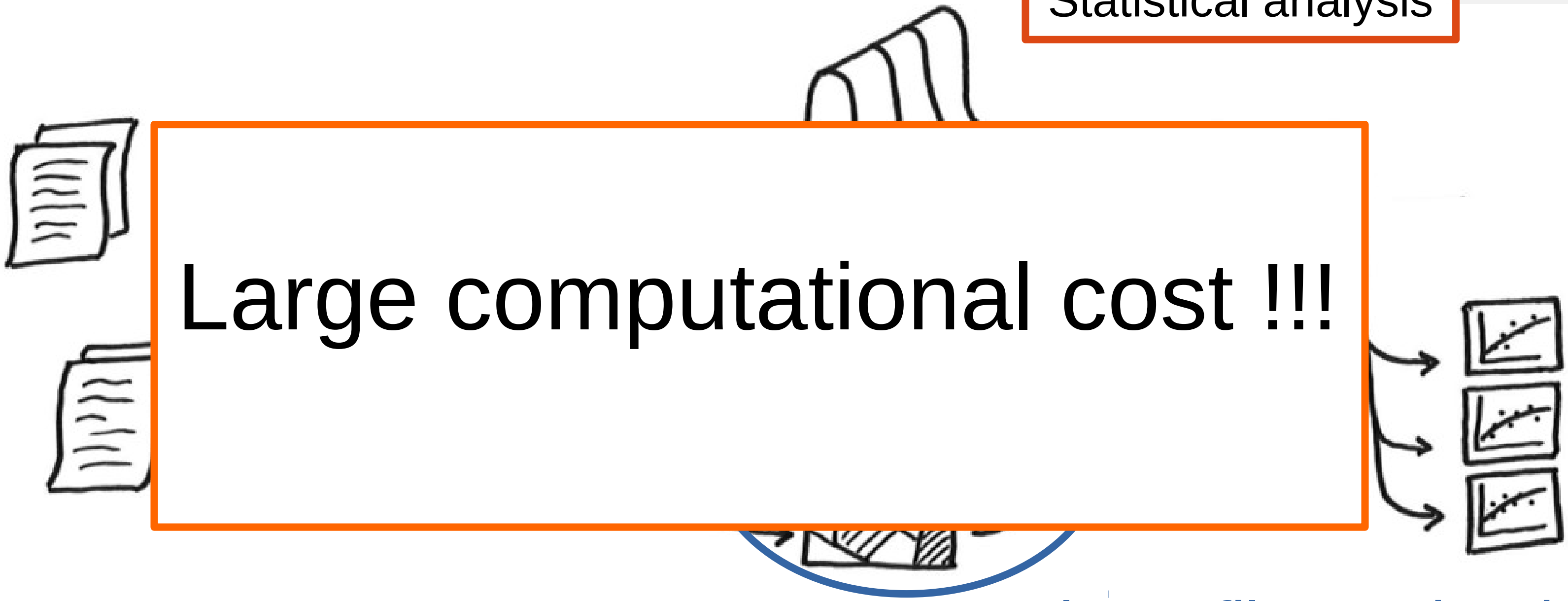
CiTIUS

Variability pipeline

Each profile → a new device needs to be simulated

Hundreds of devices

Statistical analysis



Large computational cost !!!

Apply profiles to the device

Variabililty introduced in the work-flow

CiTIUS

Variability sources

- Line edge roughness (LER)
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

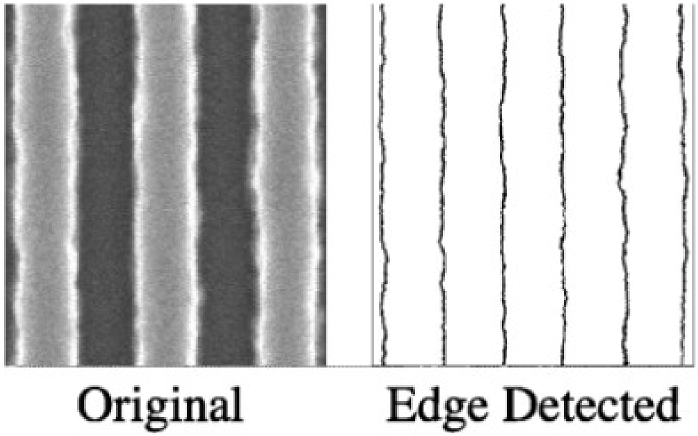
Variability sources

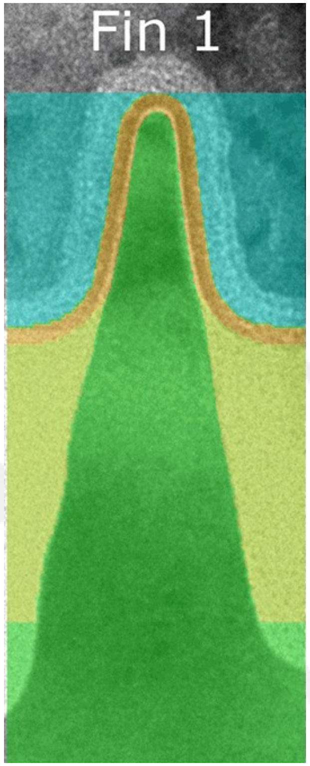
- **Line edge roughness (LER)**
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

Line-edge roughness (LER)

Motivation

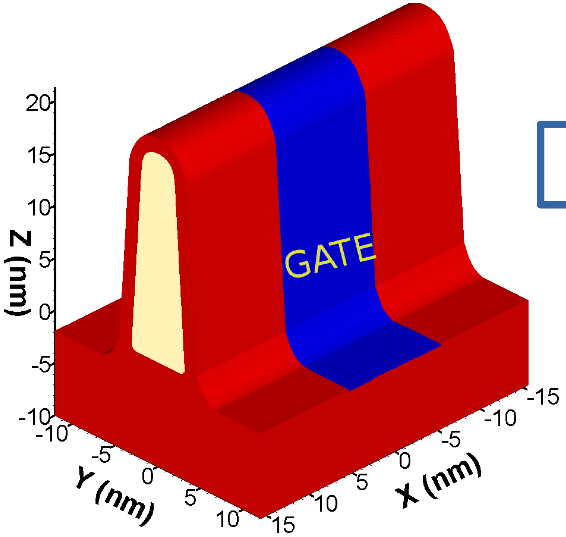
- It is **impossible** to create **straight lines** with lithography techniques
- There are **only a few atoms** of separation from the ideal device, but they make an impact.





Line-edge roughness (LER)

Modelling

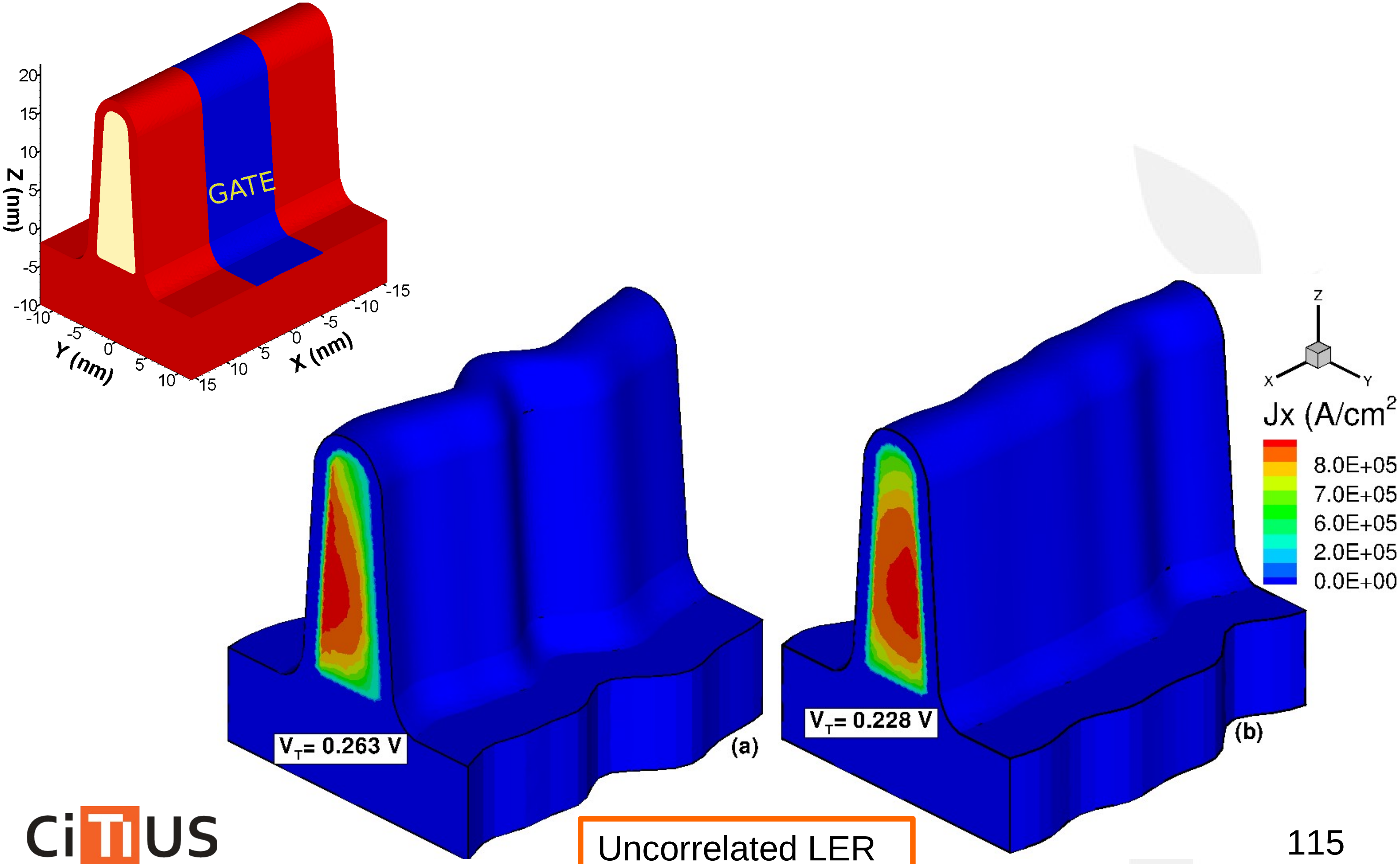


Bullet-shaped FinFET

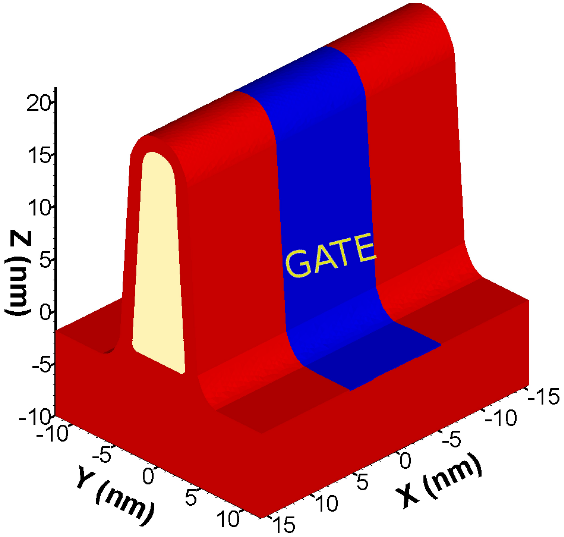
CiTIUS

Line-edge roughness (LER)

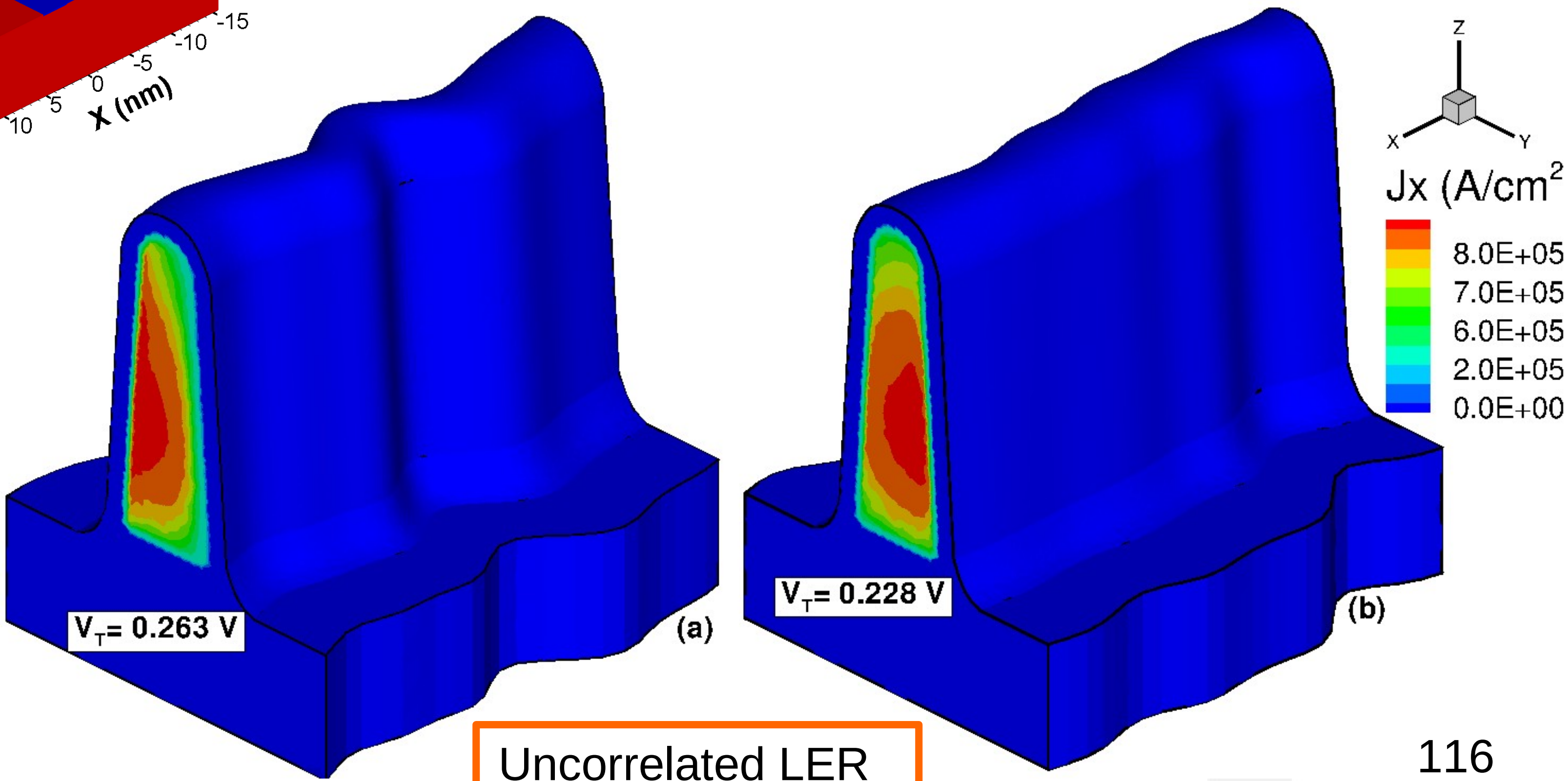
Modelling



Uncorrelated LER



Comparison of extreme cases



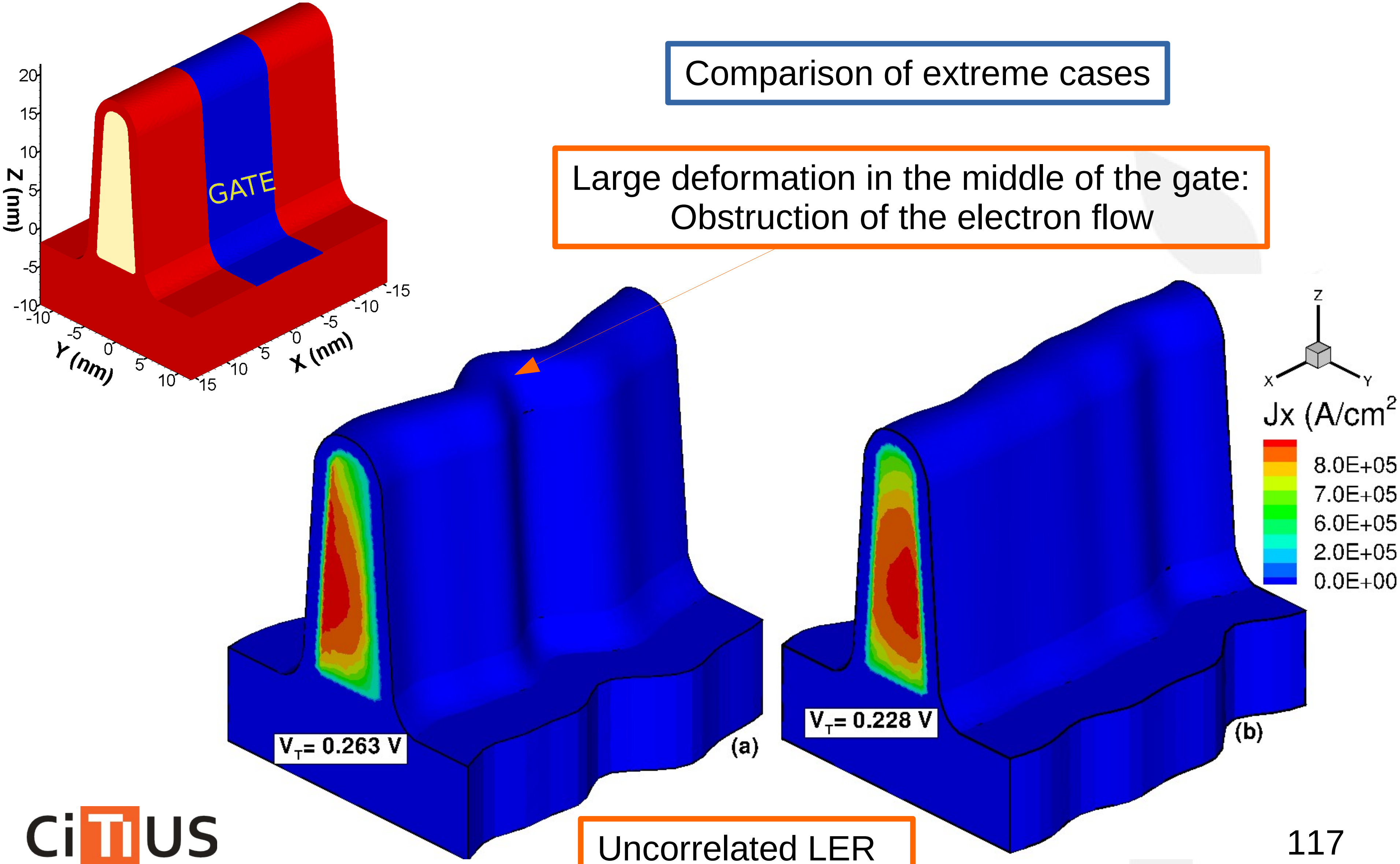
Uncorrelated LER

Line-edge roughness (LER)

Modelling

Comparison of extreme cases

Large deformation in the middle of the gate:
Obstruction of the electron flow

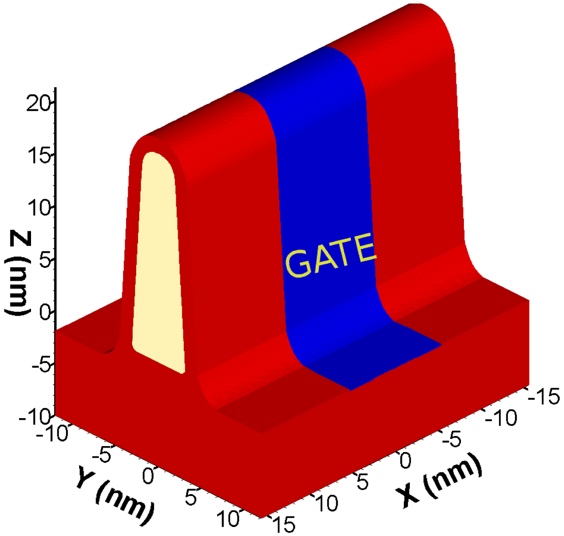


Uncorrelated LER

CiTIUS

Line-edge roughness (LER)

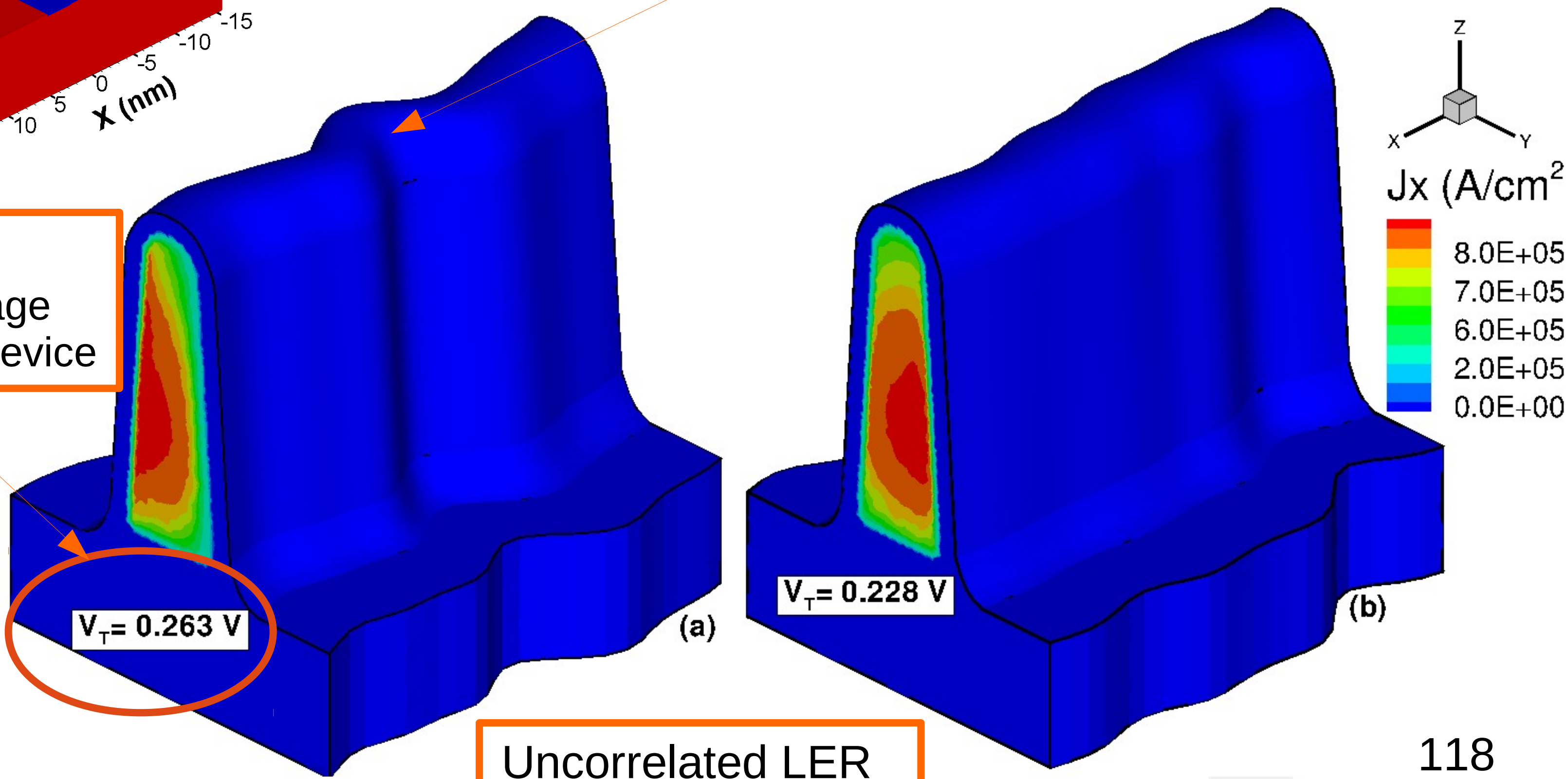
Modelling



Comparison of extreme cases

Large deformation in the middle of the gate:
Obstruction of the electron flow

Lowest I_{OFF}
large gate voltage
to turn on the device

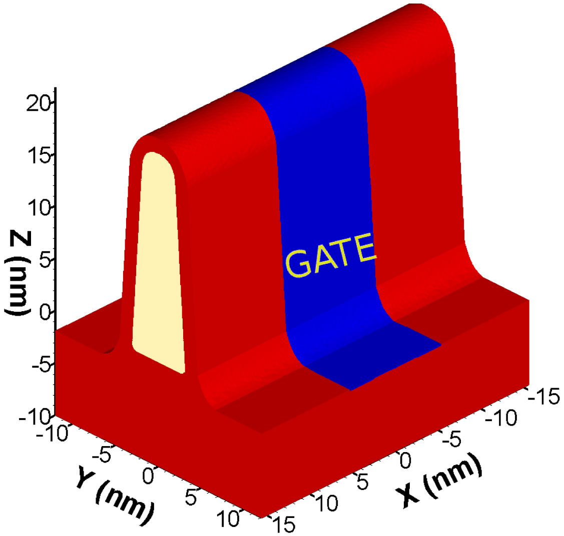


Uncorrelated LER

CiTIUS

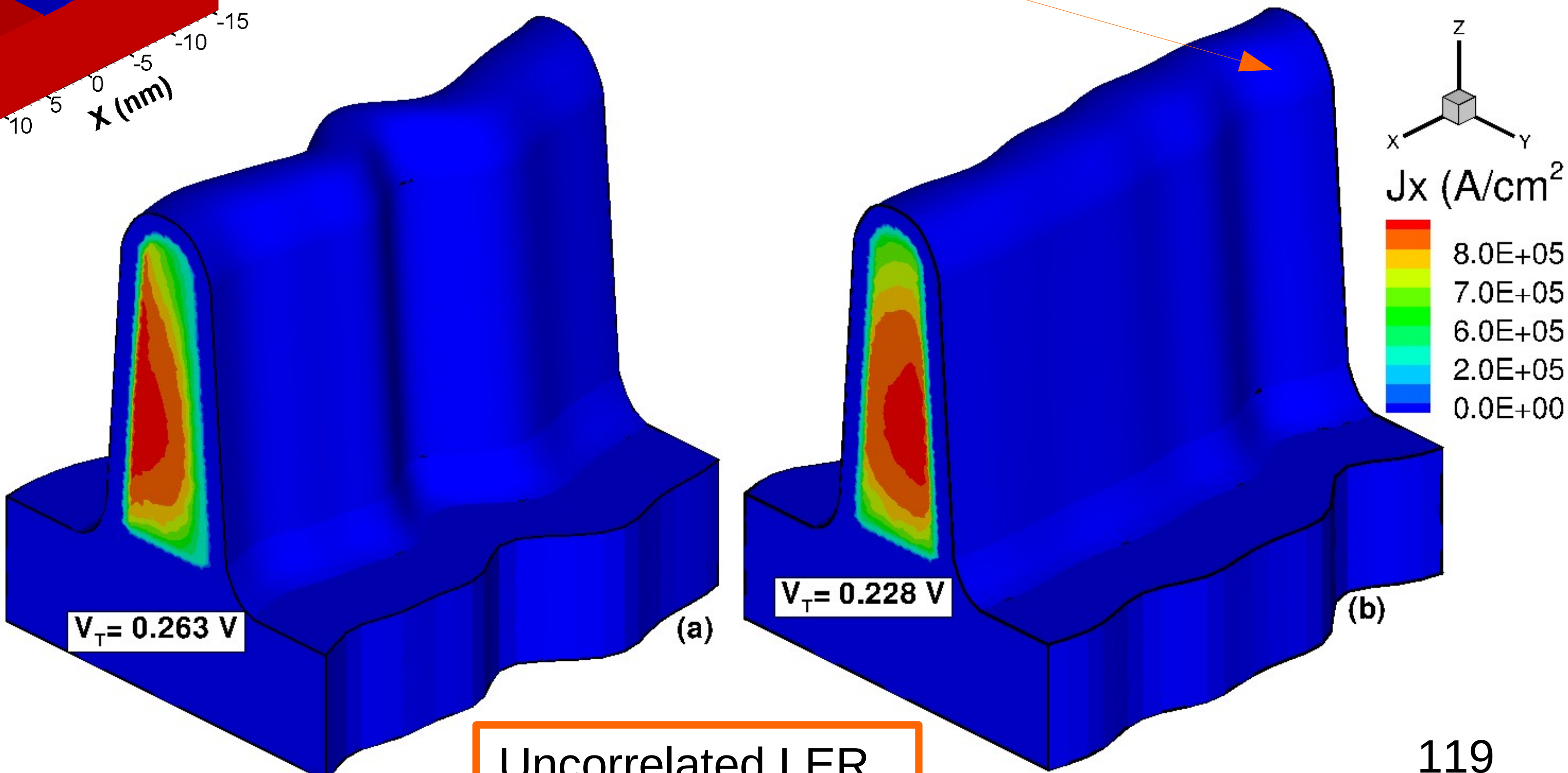
Line-edge roughness (LER)

Modelling



Comparison of extreme cases

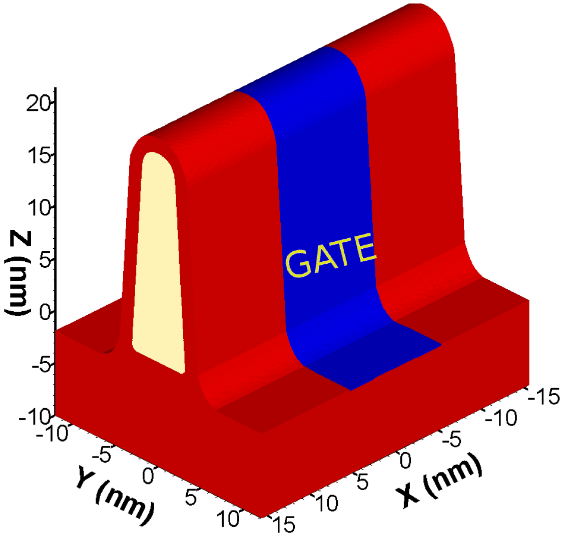
Small deformation in the drain end:
Little influence



Uncorrelated LER

Line-edge roughness (LER)

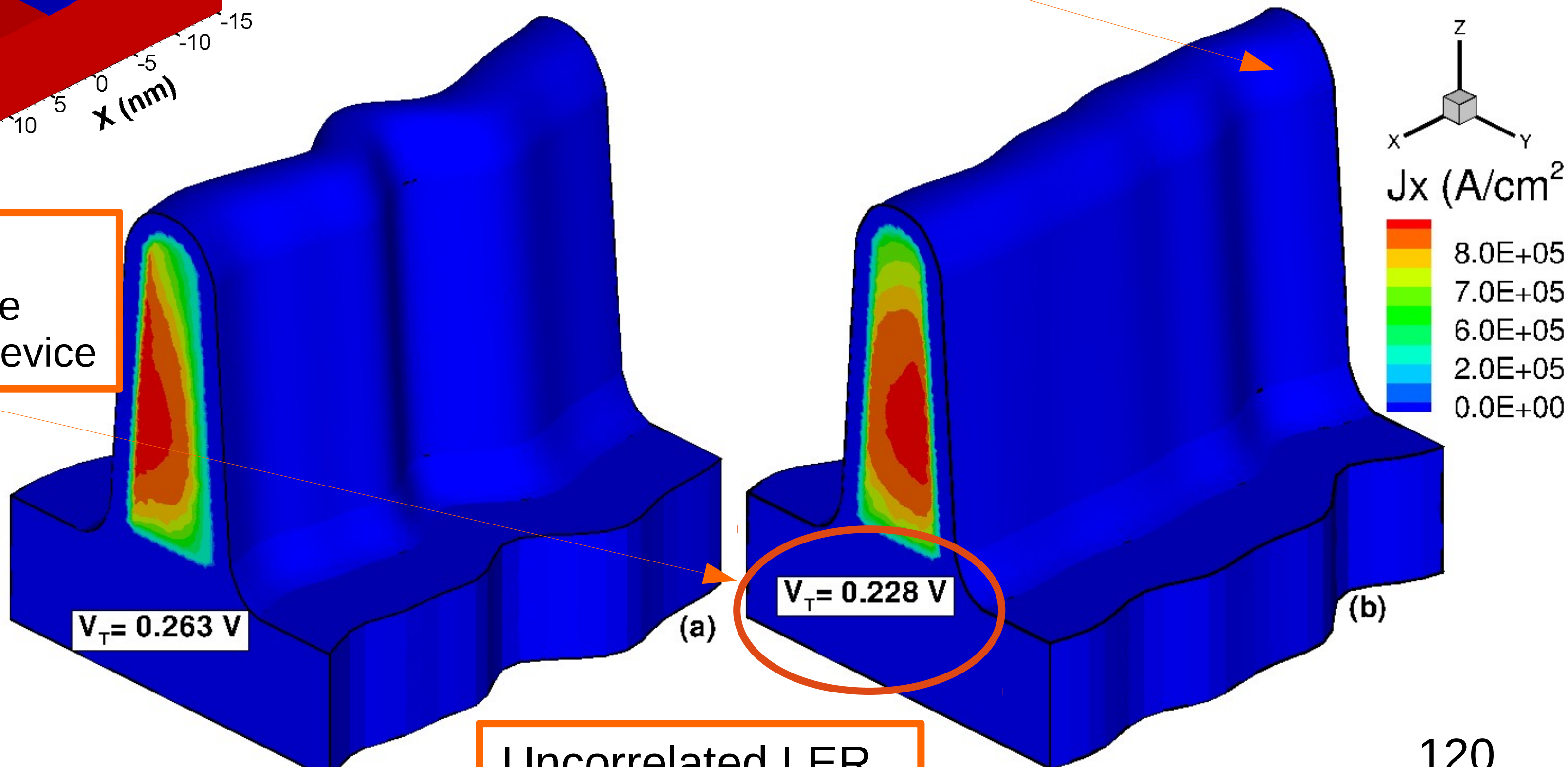
Modelling



Comparison of extreme cases

Small deformation in the drain end:
Little influence

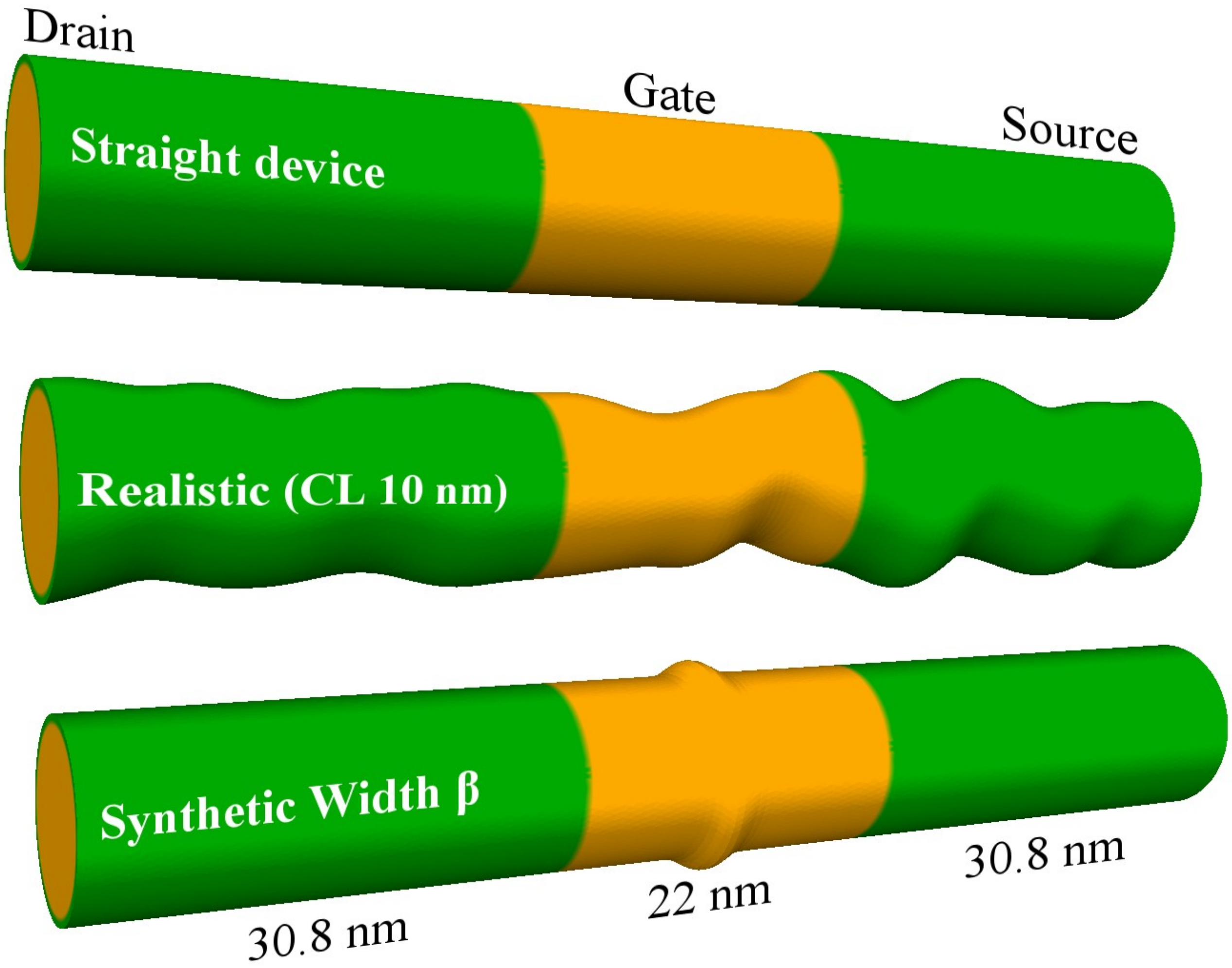
Highest I_{OFF}
low gate voltage
to turn on the device



Uncorrelated LER

Line-edge roughness (LER)

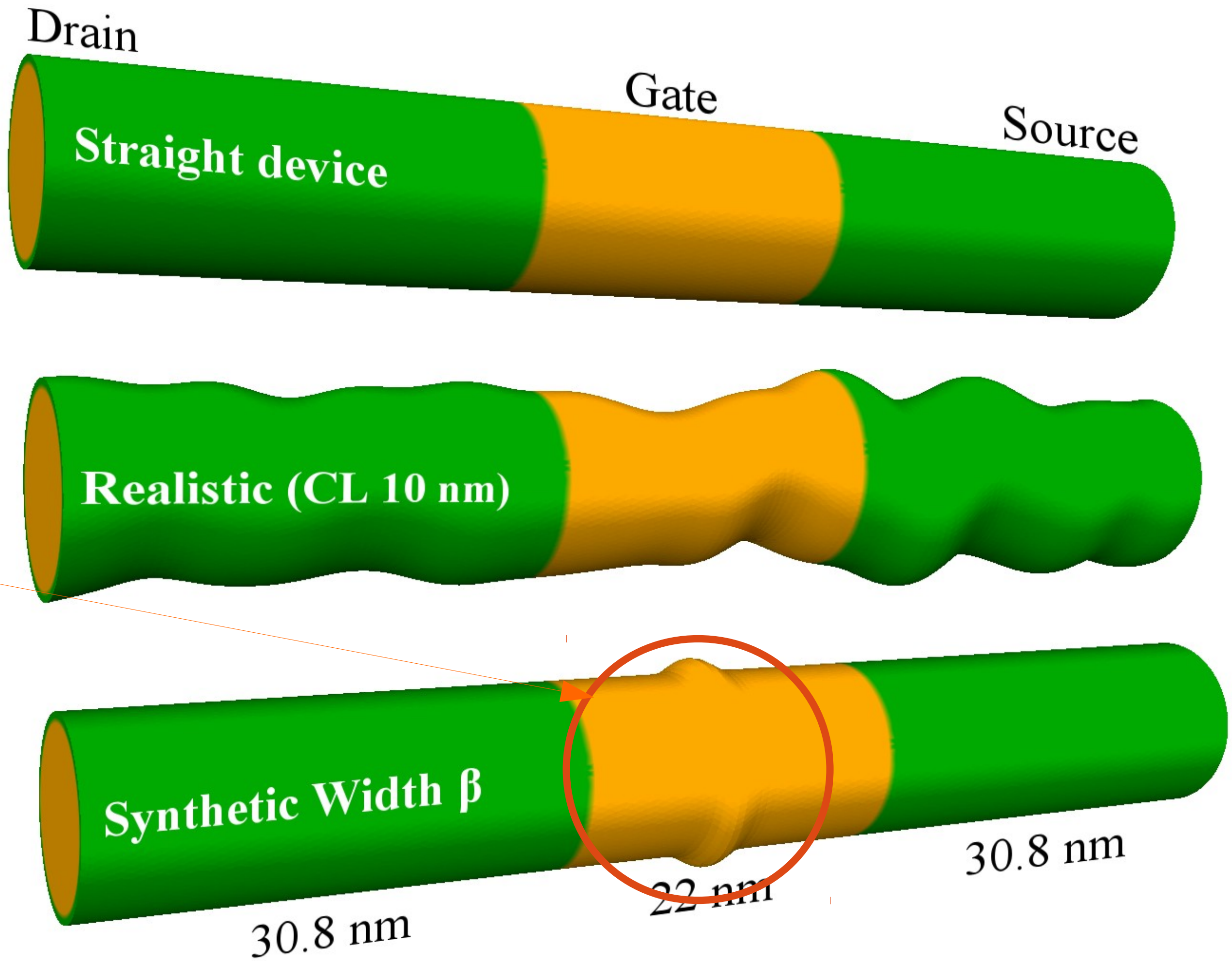
Modelling



Line-edge roughness (LER)

Modelling

Measurement of the sensitivity of a device to LER variations



Variability sources

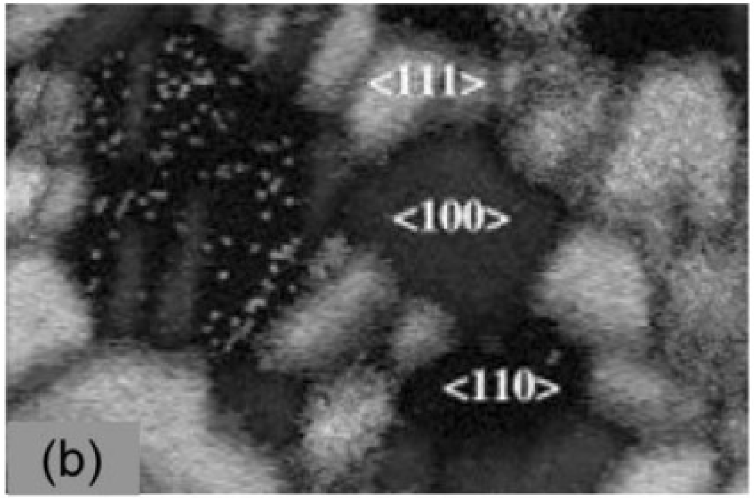
- Line edge roughness (LER)
- **Metal grain granularity (MGG)**
- Random dopants (RD)
- Defects in high-k dielectrics

CiTIUS

Metal grain granularity (MGG)

Motivation

- **Metals** used as **gate contacts** present crystallographic domains (grains)
- **Lithography** processes can create even **bigger grains**, increasing the effect of the variability source
- These grains have **different work-function values** and **orientations**



CiTIUS

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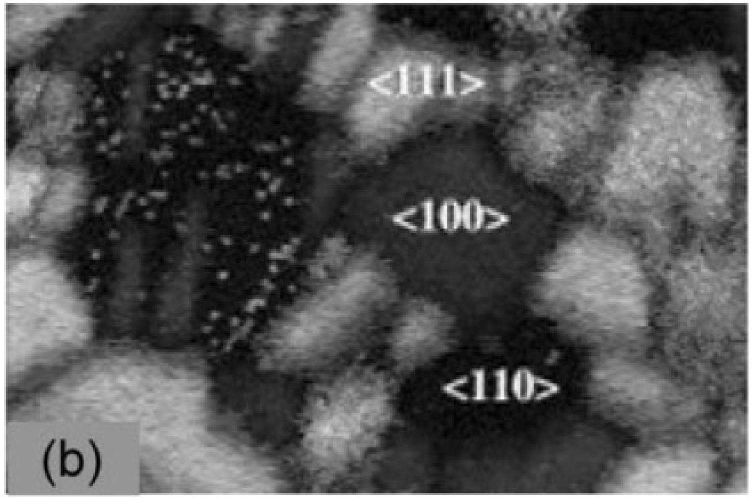
Key to control the gate of the device



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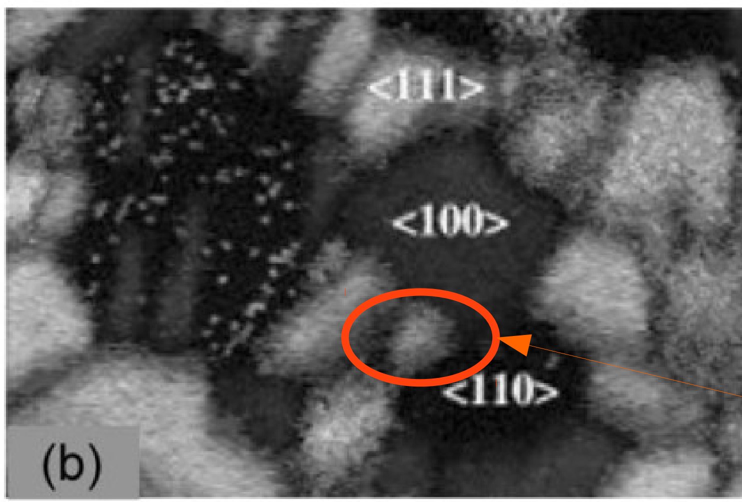
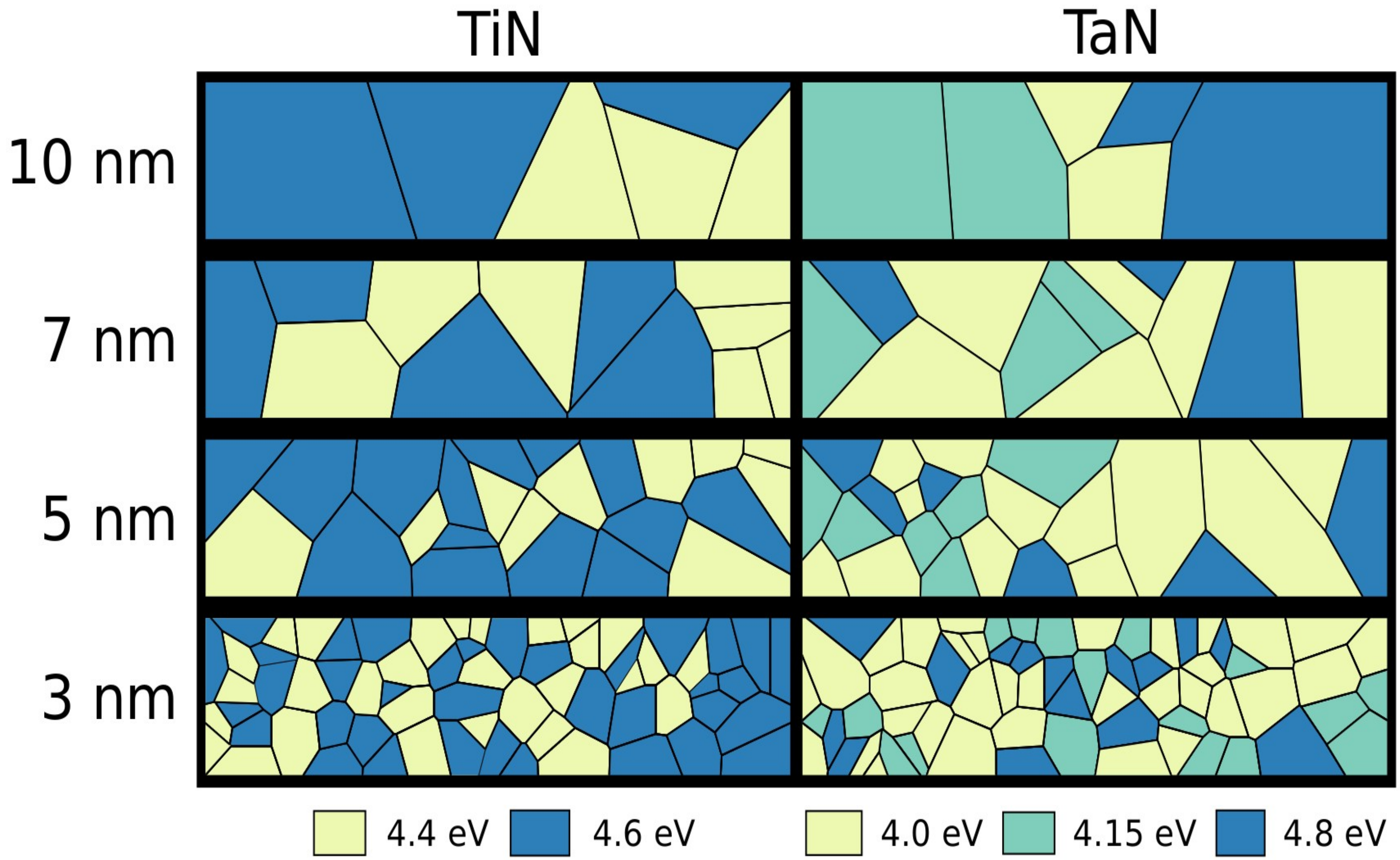


The grain size can also change

Metal grain granularity (MGG)

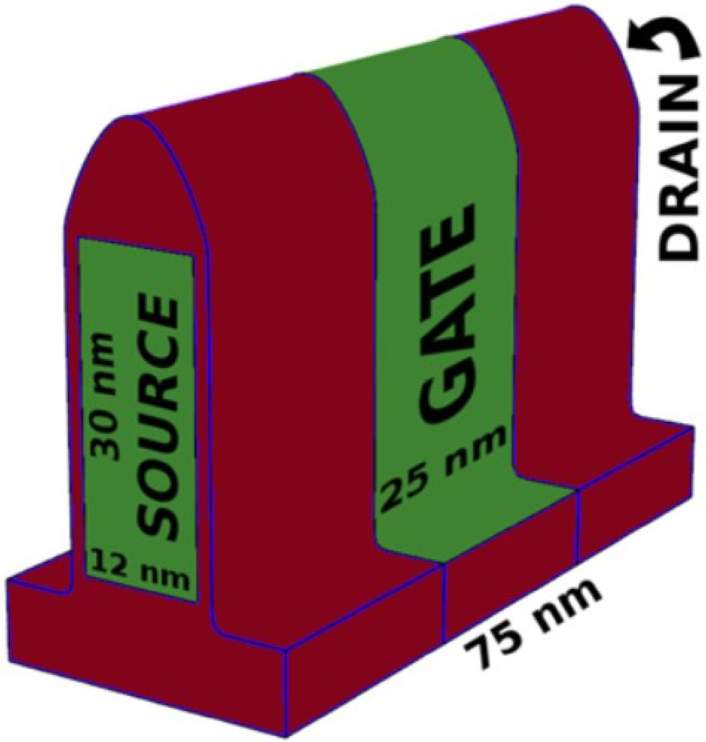
Modelling



Voronoi approach to create the **MGG**

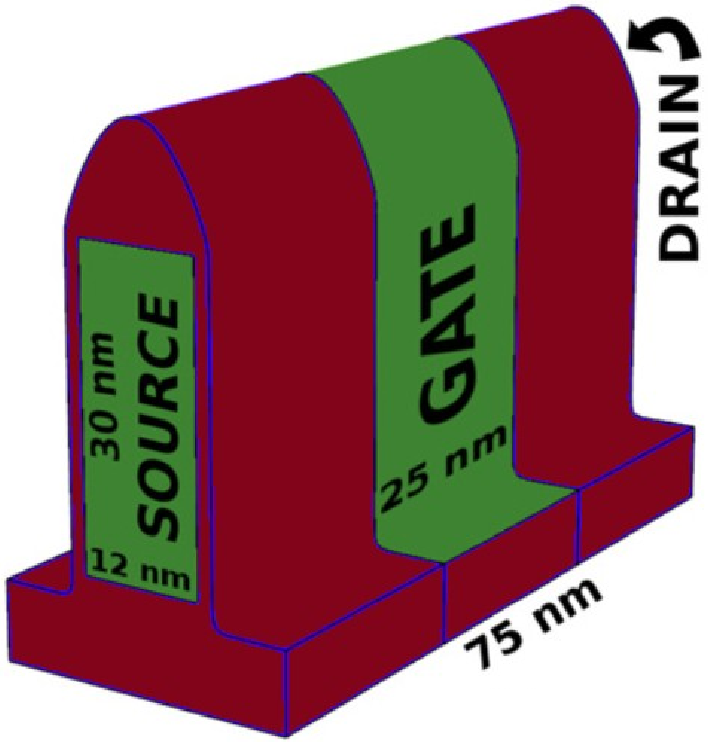
Metal grain granularity (MGG)

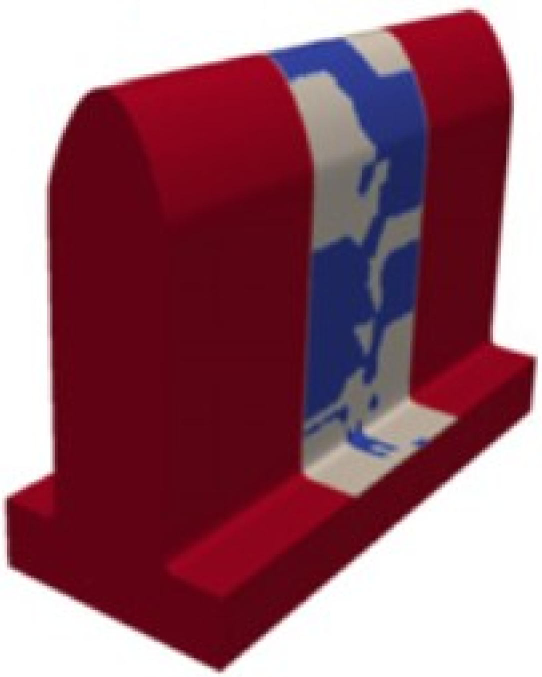
Modelling



Metal grain granularity (MGG)

Modelling

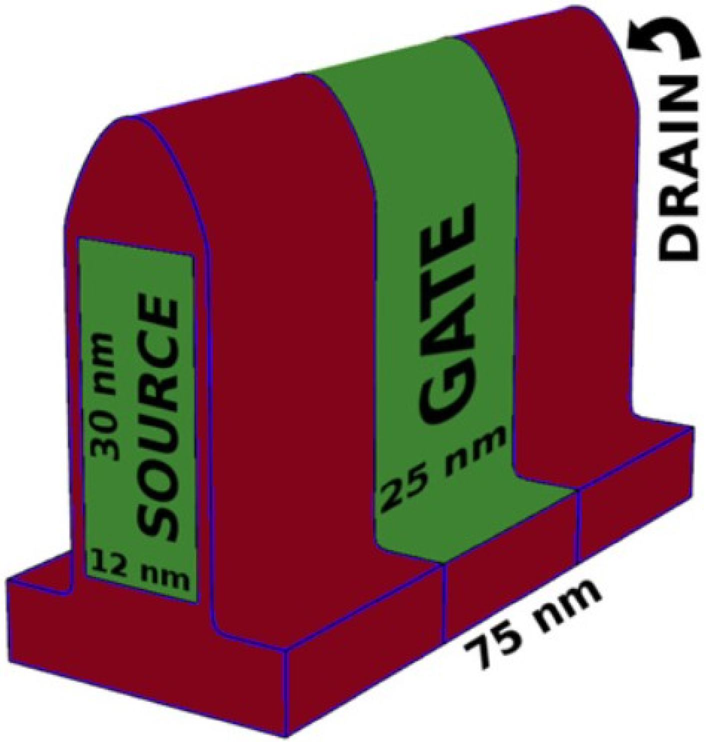


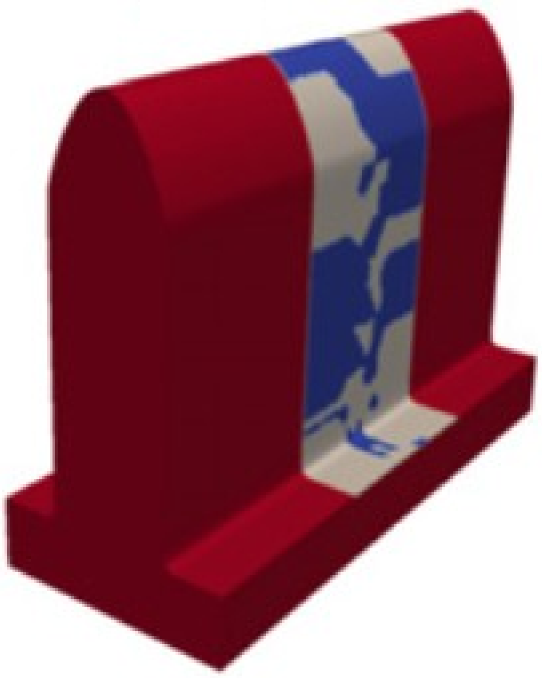


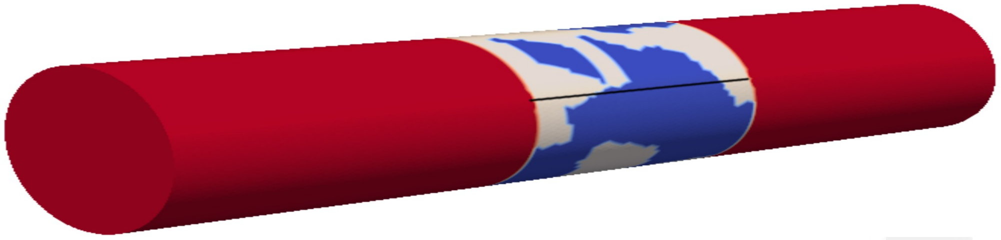
CiTIUS

Metal grain granularity (MGG)

Modelling





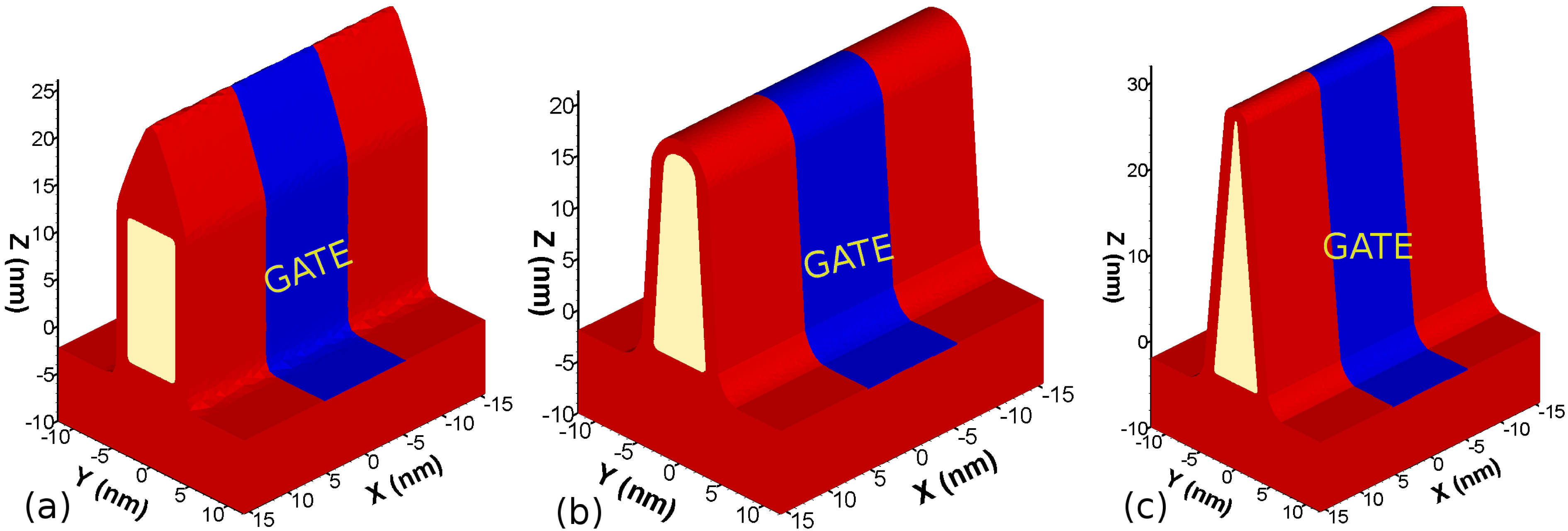


CiTIUS

MGG: What's happening inside the device?

10.4 nm gate length InGaAs FinFET devices

Rectangular (REC)	Bullet-shaped (BUL)	Triangular (TRI)

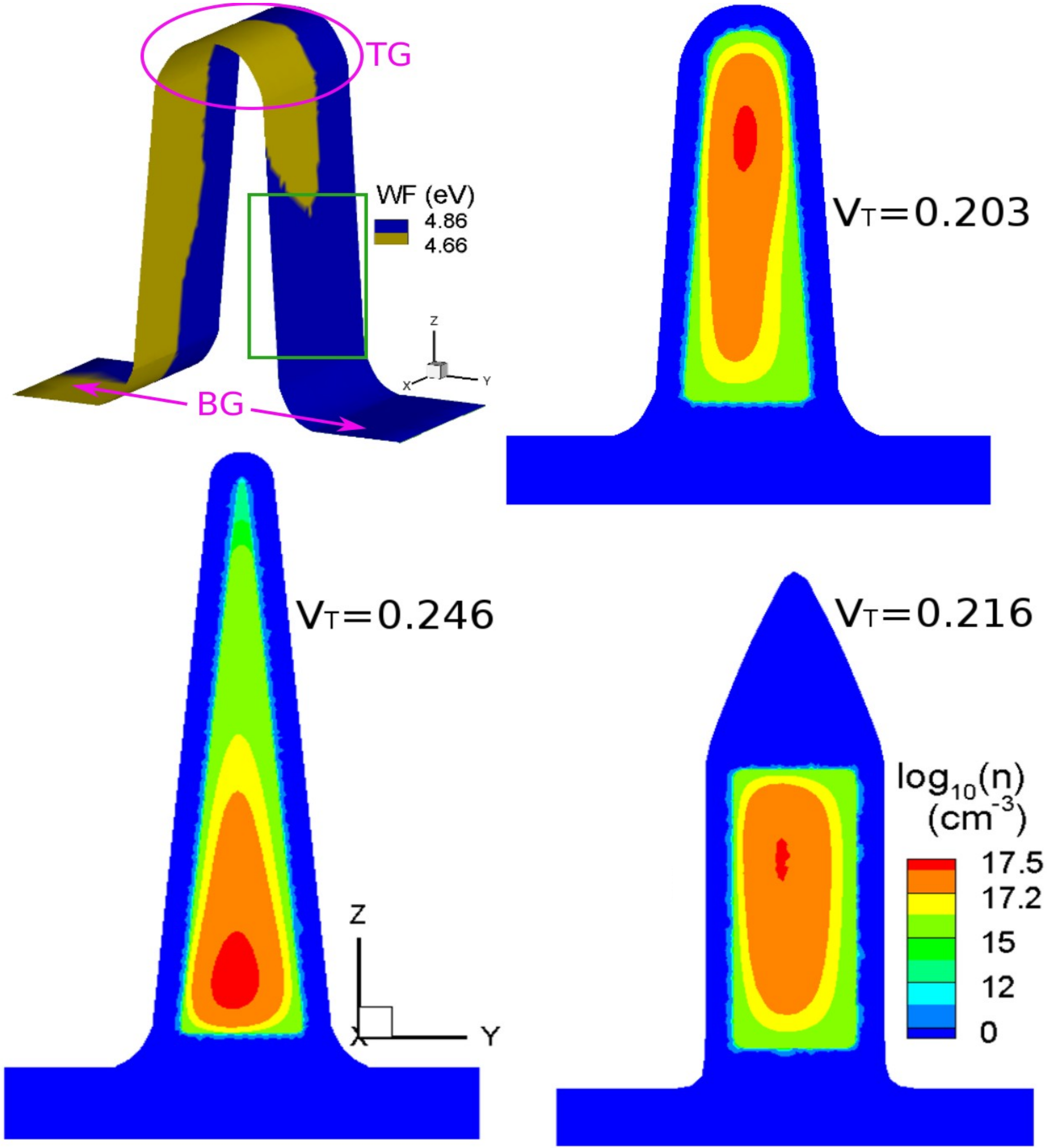


We apply a MGG profile
Cut in the middle of the gate (X=0 nm)

CiTIUS

MGG: What's happening inside the device?

Electron density cross-section in the middle of the gate

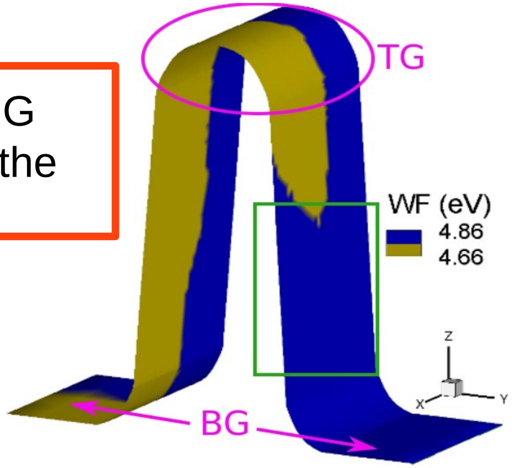


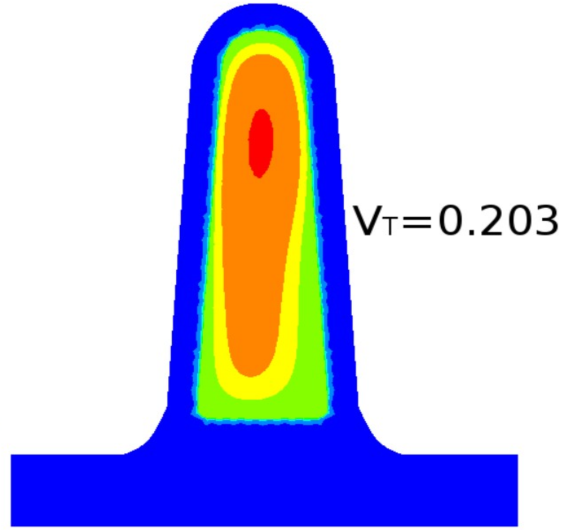
CiTIUS

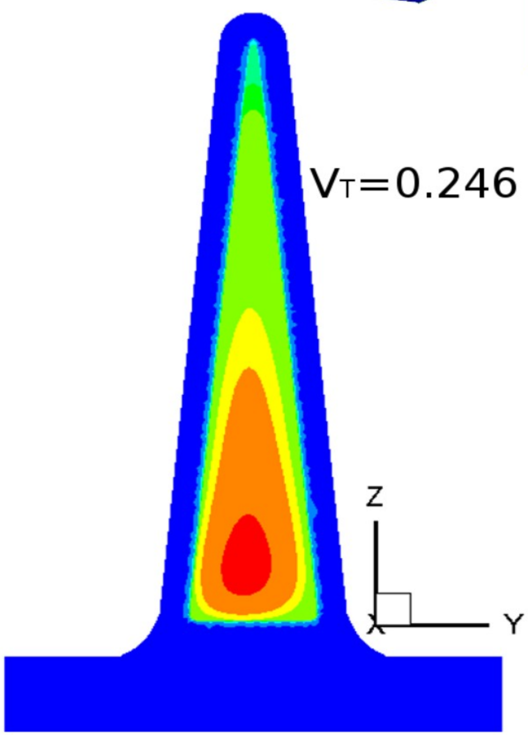
MGG: What's happening inside the device?

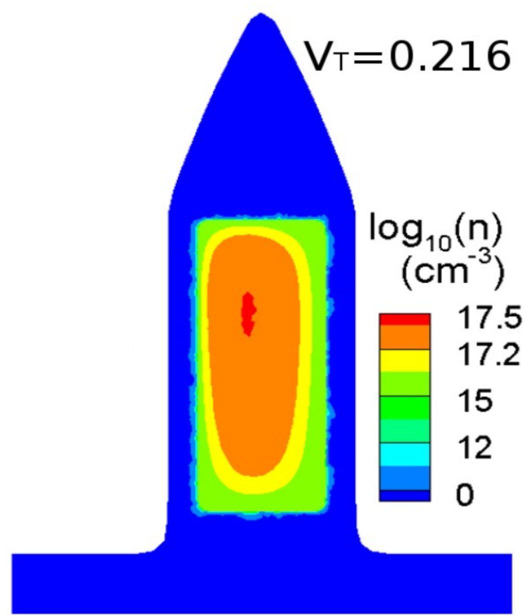
Electron density cross-section in the middle of the gate

Example of a MGG profile applied to the TiN metal gate







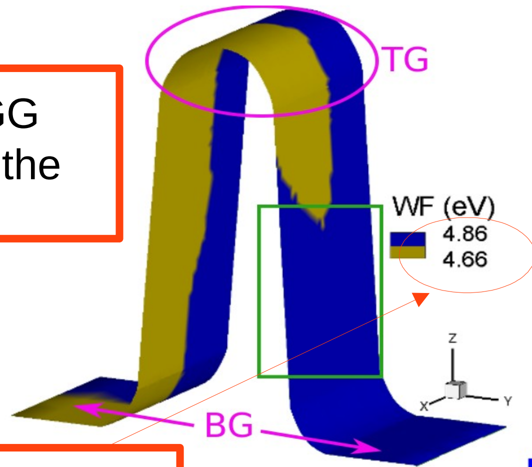


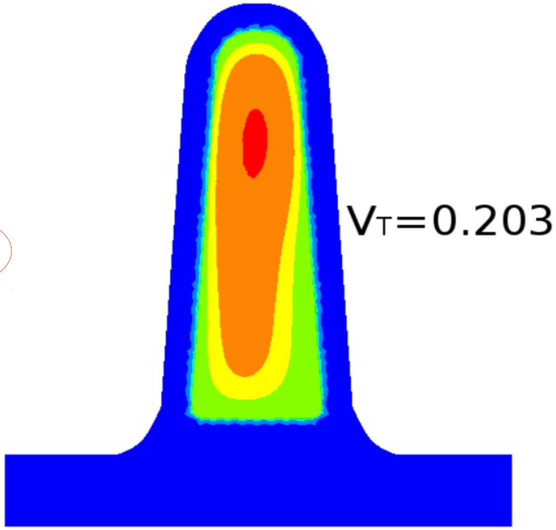
CiTIUS

MGG: What's happening inside the device?

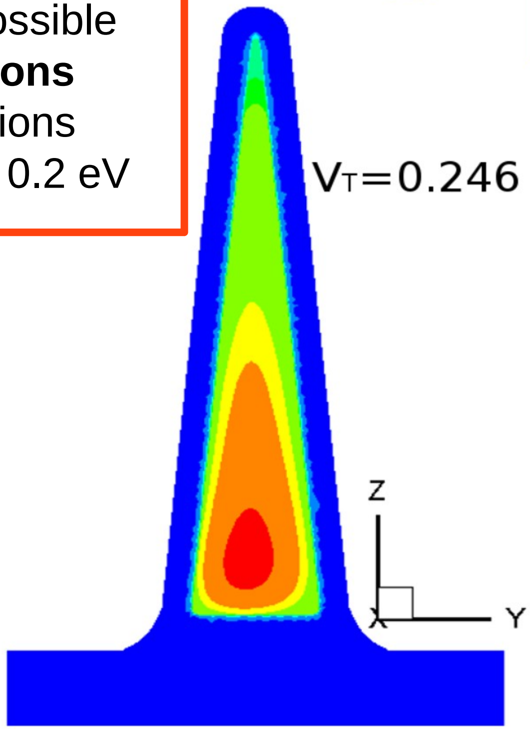
Electron density cross-section in the middle of the gate

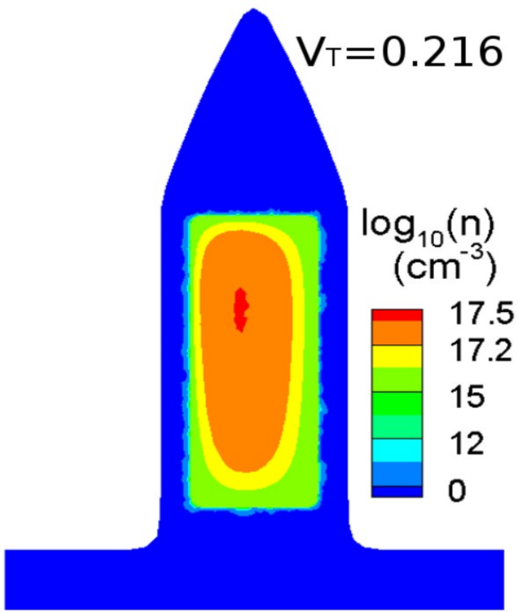
Example of a MGG profile applied to the TiN metal gate





TiN has **two** possible **grain orientations** with work functions (WF) spanning 0.2 eV



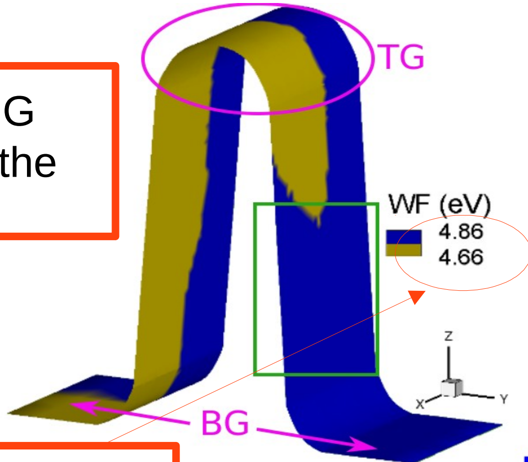


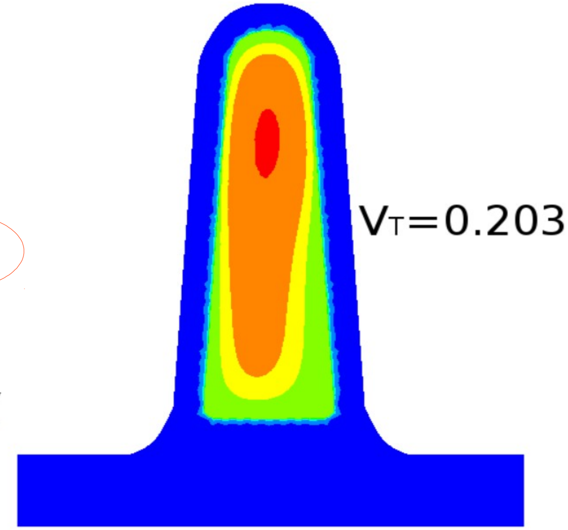
CiTIUS

MGG: What's happening inside the device?

Electron density cross-section in the middle of the gate

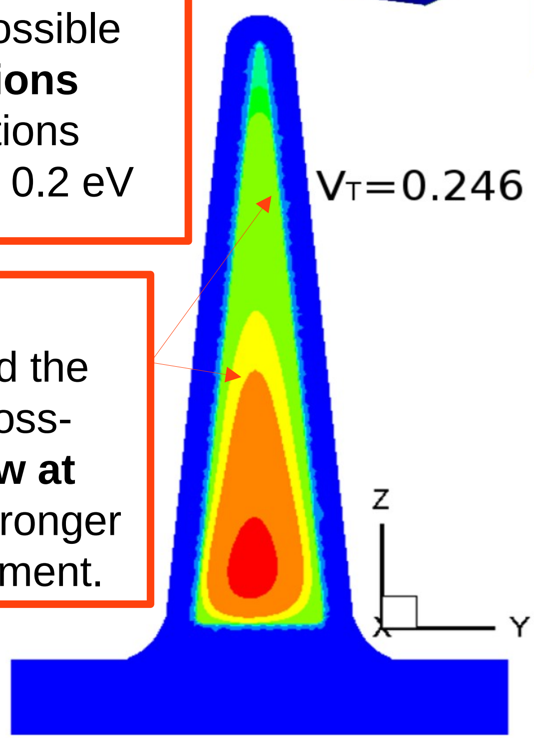
Example of a MGG profile applied to the TiN metal gate

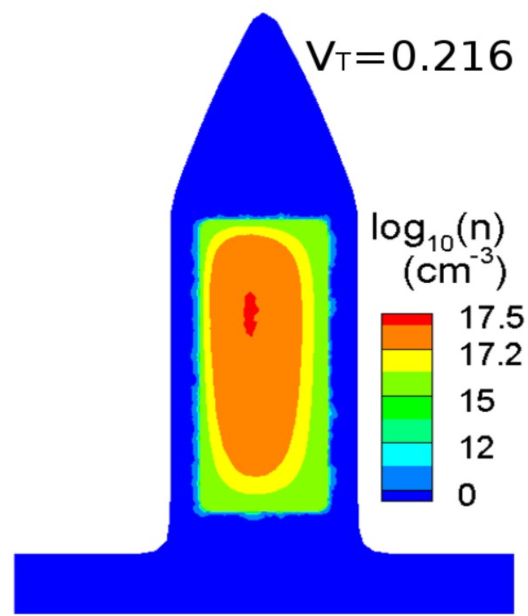




TiN has **two** possible **grain orientations** with work functions (WF) spanning 0.2 eV

TRI: **density** distributed toward the **bottom** of the cross-section and is **low at the top** due to stronger quantum confinement.



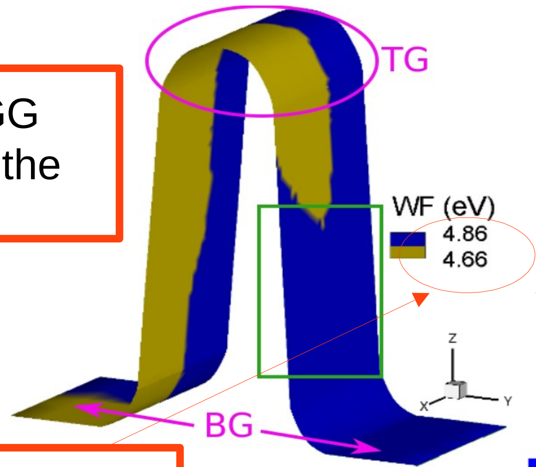


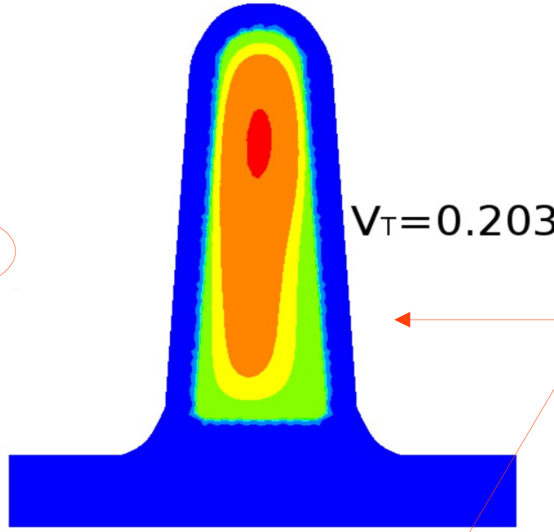
CiTIUS

MGG: What's happening inside the device?

Electron density cross-section in the middle of the gate

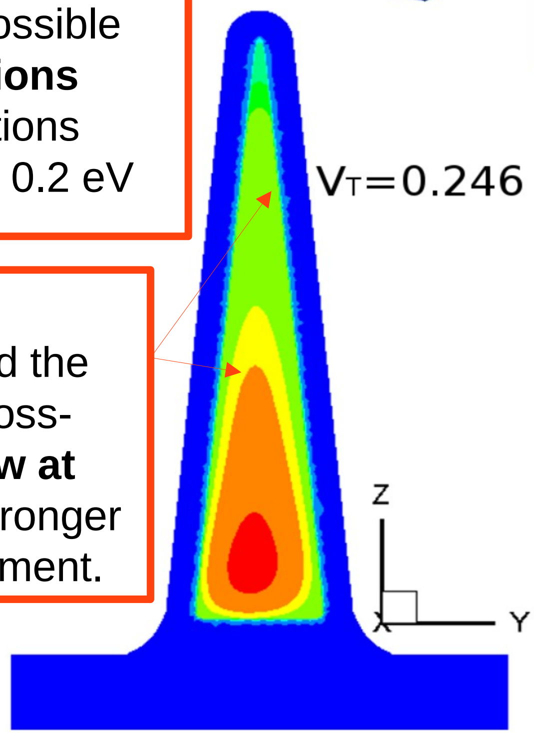
Example of a MGG profile applied to the TiN metal gate

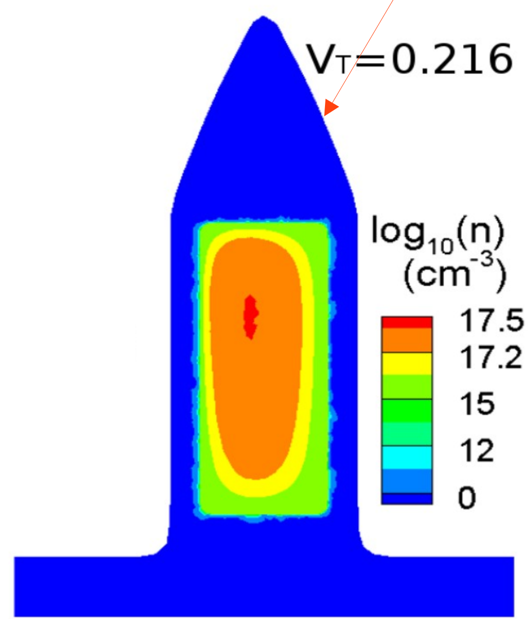




REC and **BUL**: **density** distributed along the **entire channel**, but the **larger** values are found at the **top** of the cross-section.

TiN has **two** possible **grain orientations** with work functions (WF) spanning 0.2 eV





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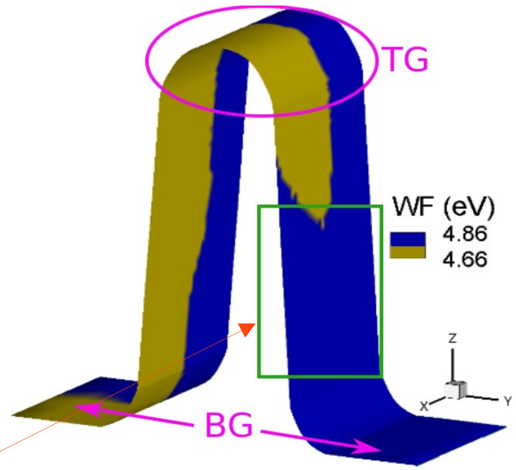
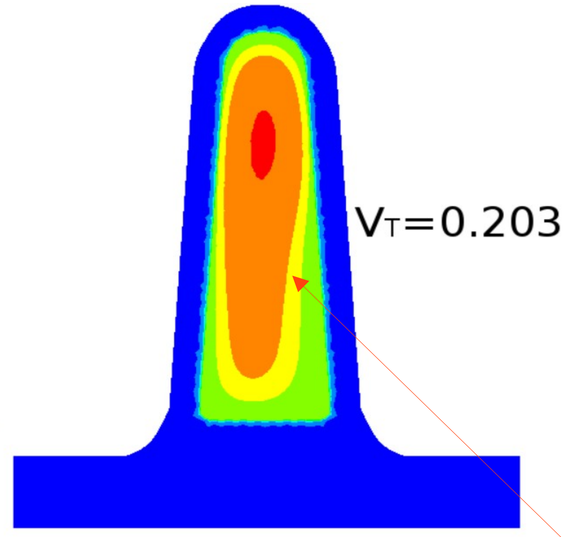
CiTIUS

MGG: What's happening inside the device?

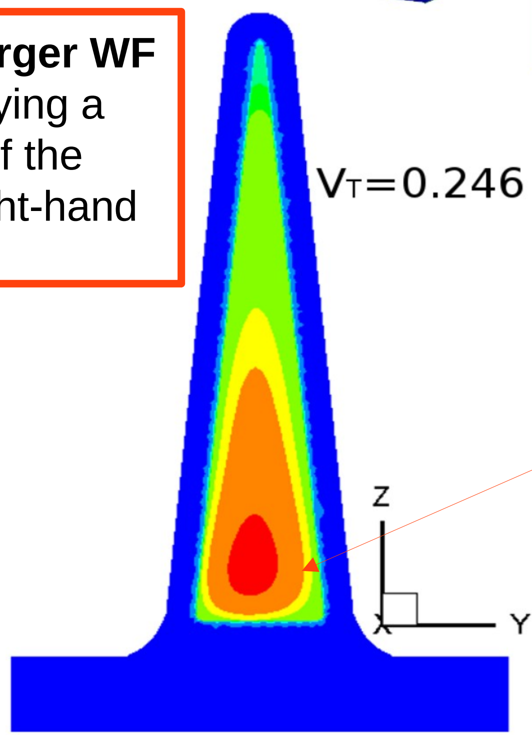
Electron density cross-section in the middle of the gate

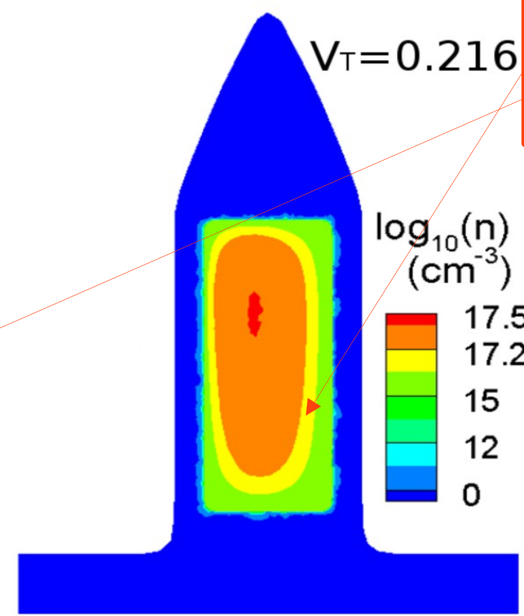




Grains with a **larger WF** value are occupying a significant part of the **gate** profile's right-hand side

which is **pushing** the **electron density** to the **opposite side** of the device





CiTIUS

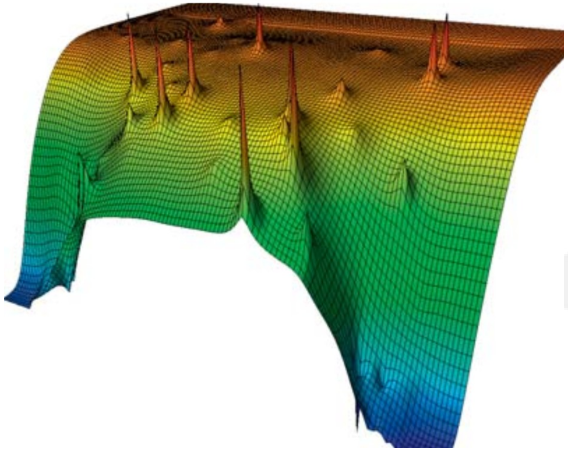
Variability sources

- Line edge roughness (LER)
- Metal grain granularity (MGG)
- **Random dopants (RD)**
- Defects in high-k dielectrics

Random dopants (RD)

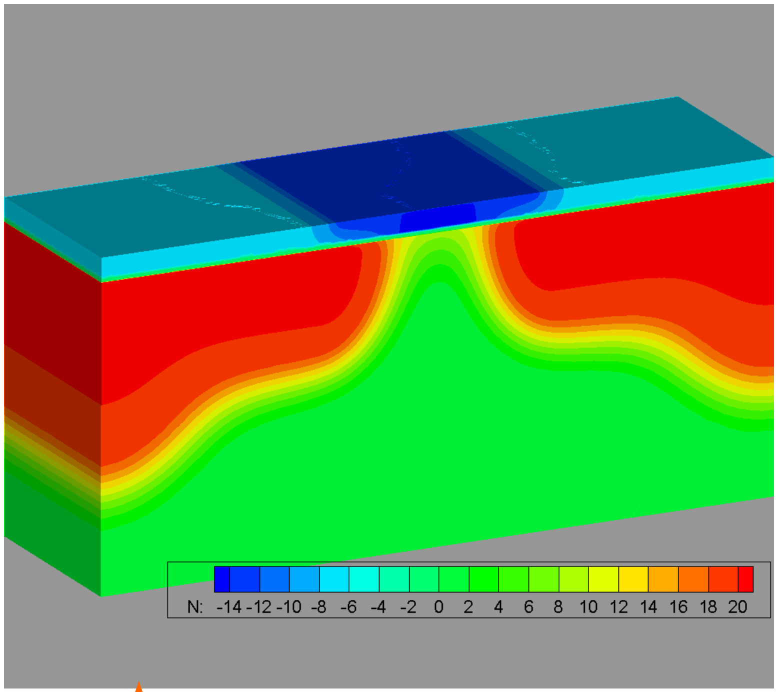
Motivation

- It is **impossible** to **predict** how the atomic **dopants**' atoms will be arranged within the transistors
- This leads to **variations** in the current flow and **disruptions**



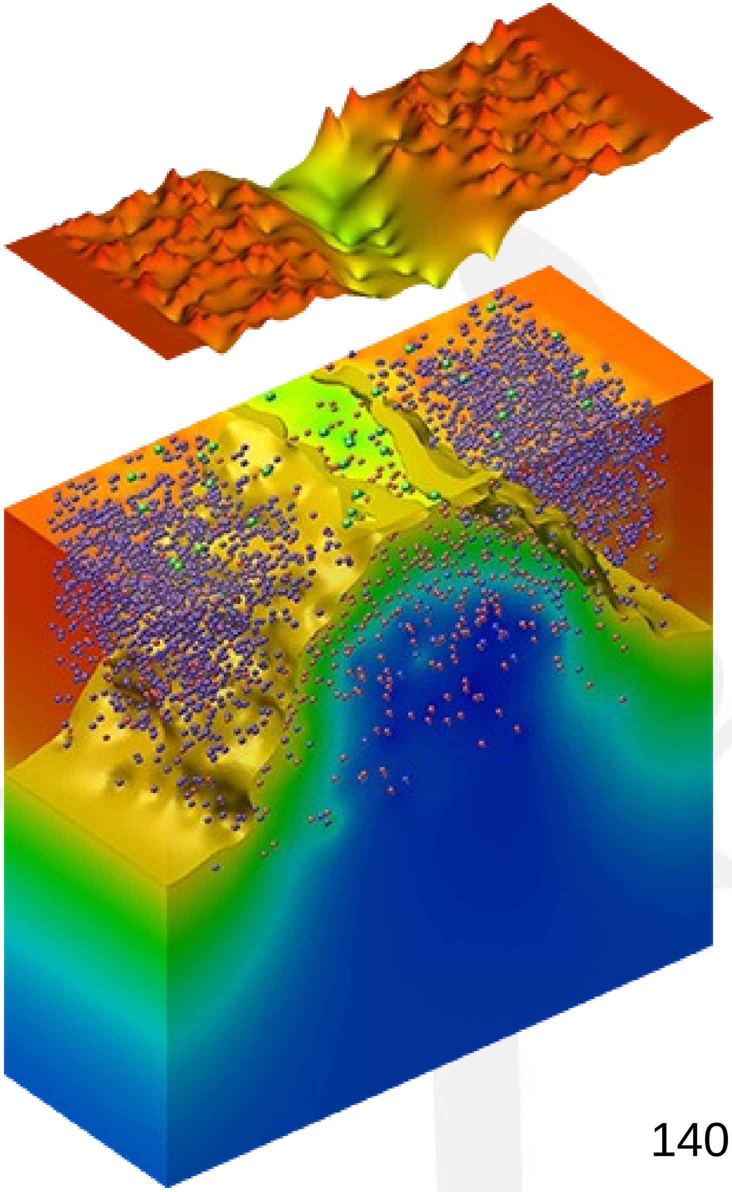
Random dopants (RD)

Modelling



Continuous doping values

Individual impurity atoms



CiTIUS

Random dopants (RD)

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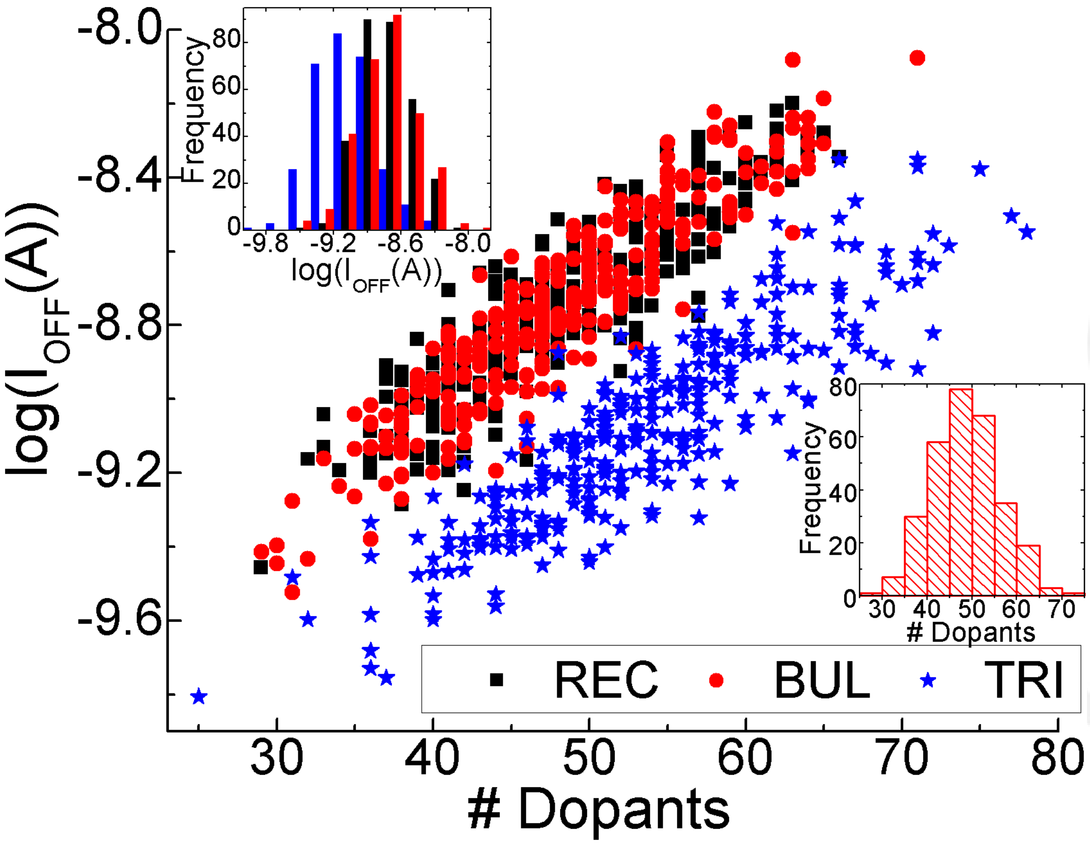

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Defects in high-k dielectrics

Motivation

- Under **high temperatures** annealings, high-k materials become **polycrystalline**
- Variations of the **oxide thickness** and **charge trapping** can affect the properties of the scaled devices

CiTIUS

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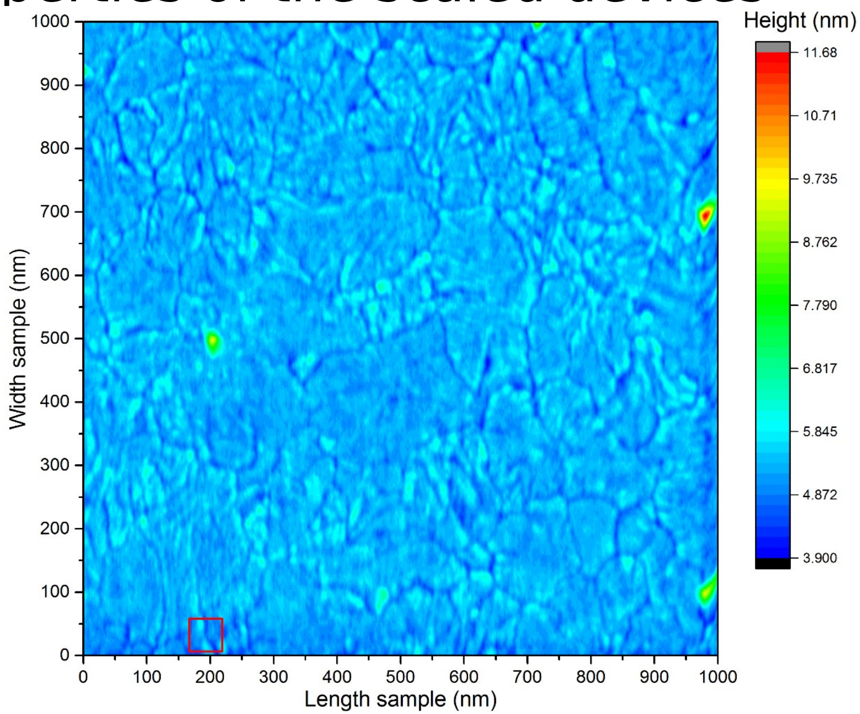
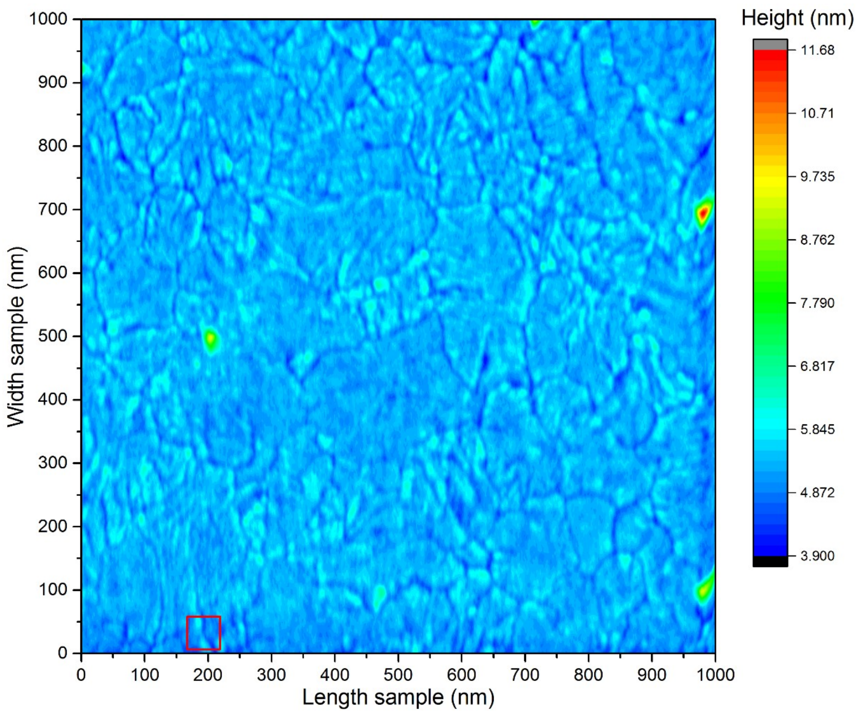


Experimental data measured in the Universitat Autónoma de Barcelona

Defects in high-k dielectrics

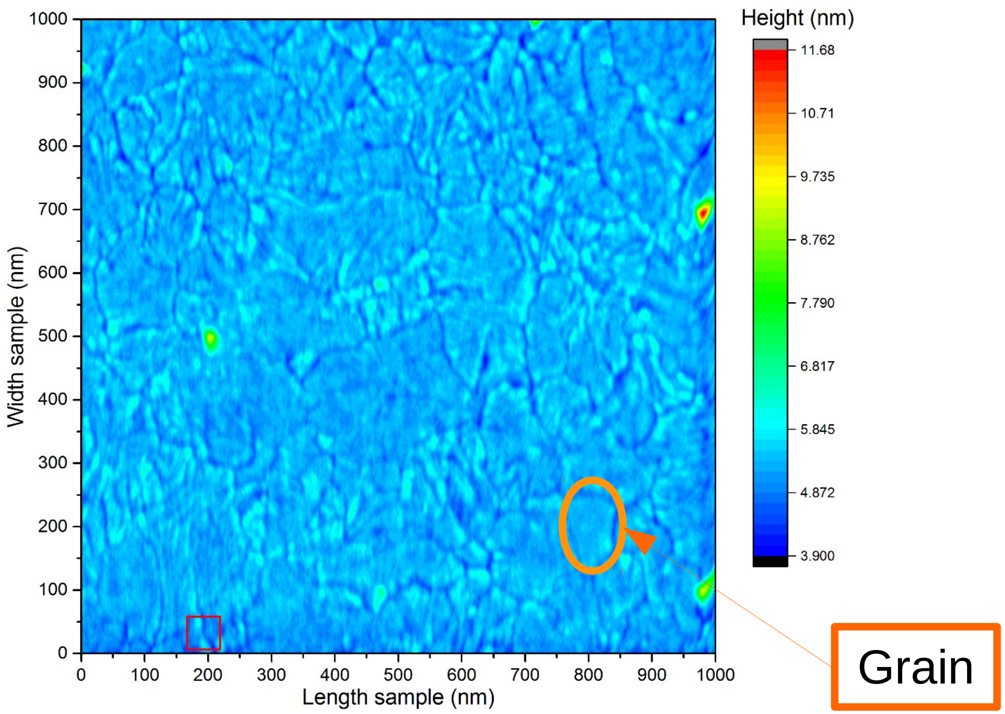
Motivation



Topography map obtained at V_G=6.5V on a HfO_2/SiO_2/p-Si structure (250 nm x 300 nm)

Defects in high-k dielectrics

Motivation



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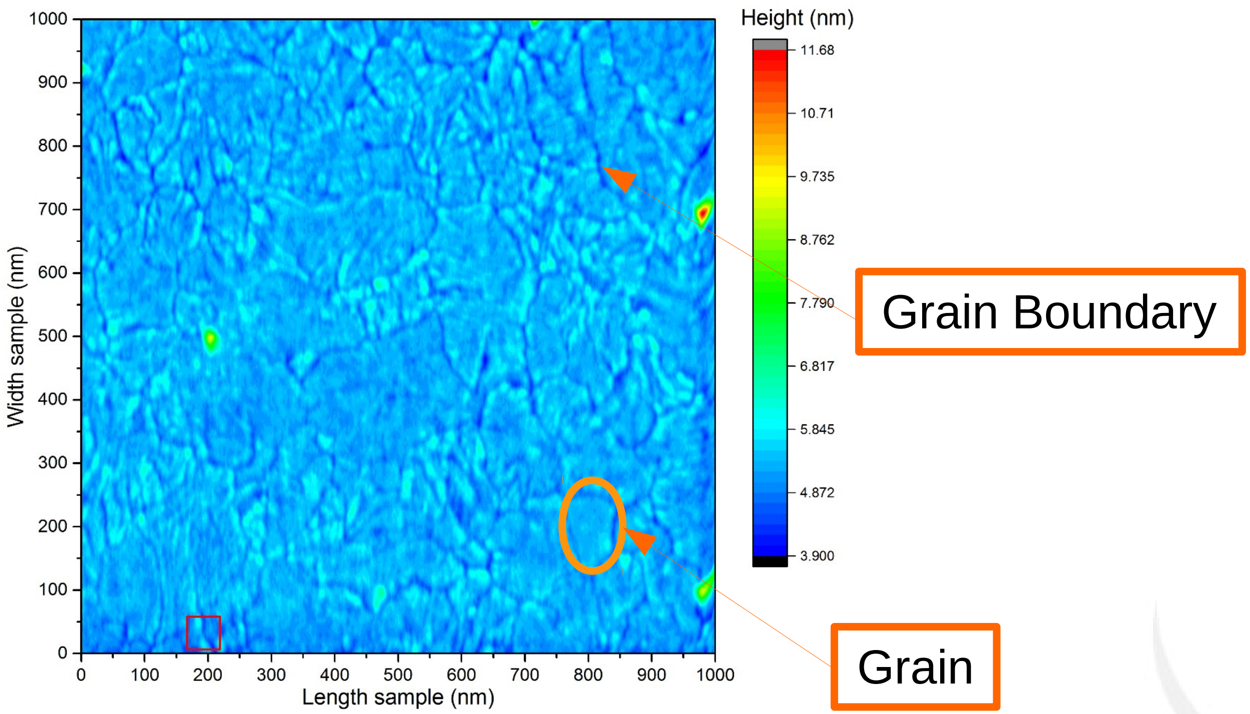

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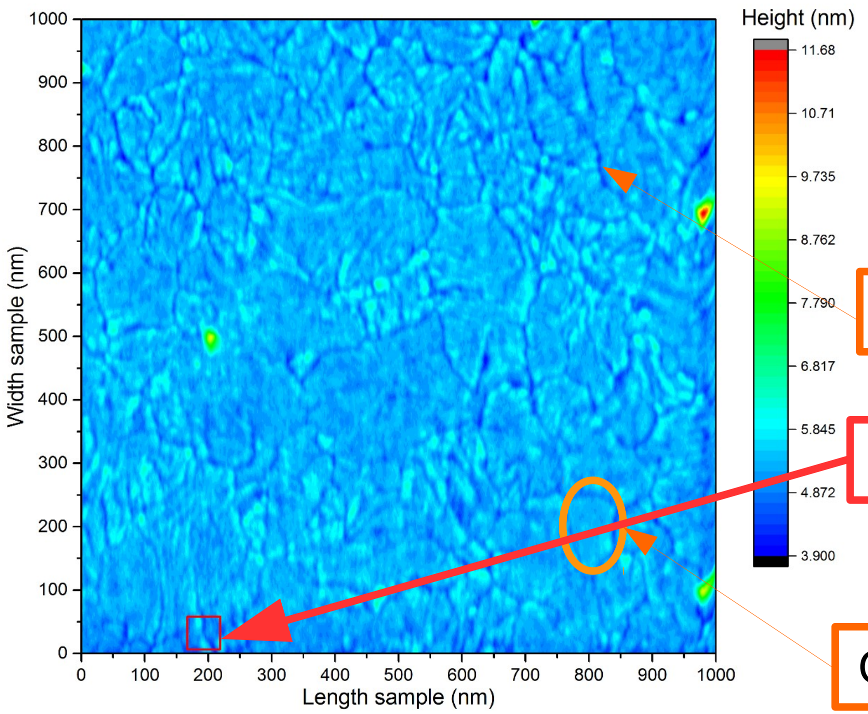
CiTIUS

Defects in high-k dielectrics

Motivation



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CiTIUS

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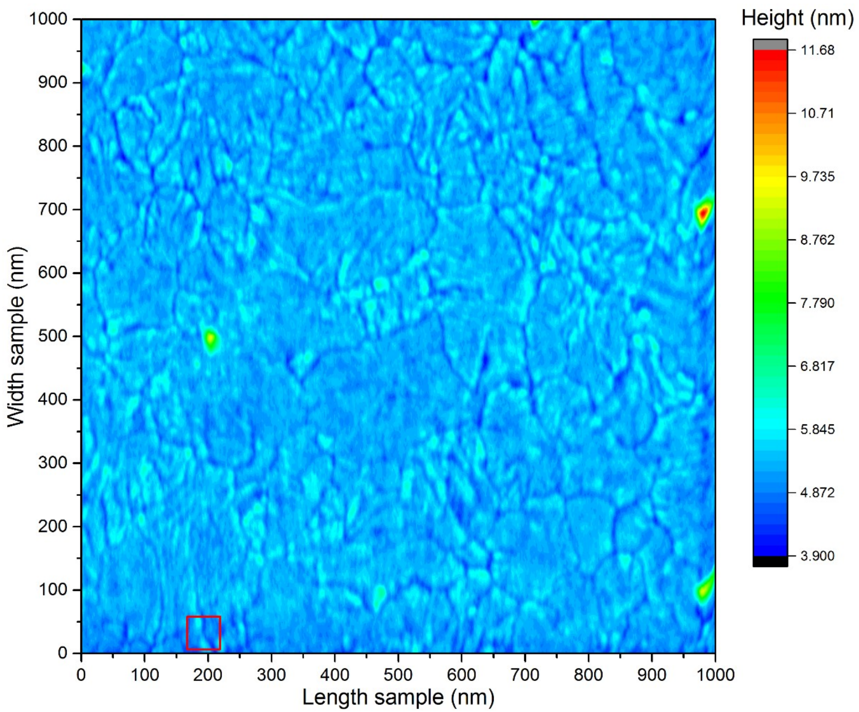

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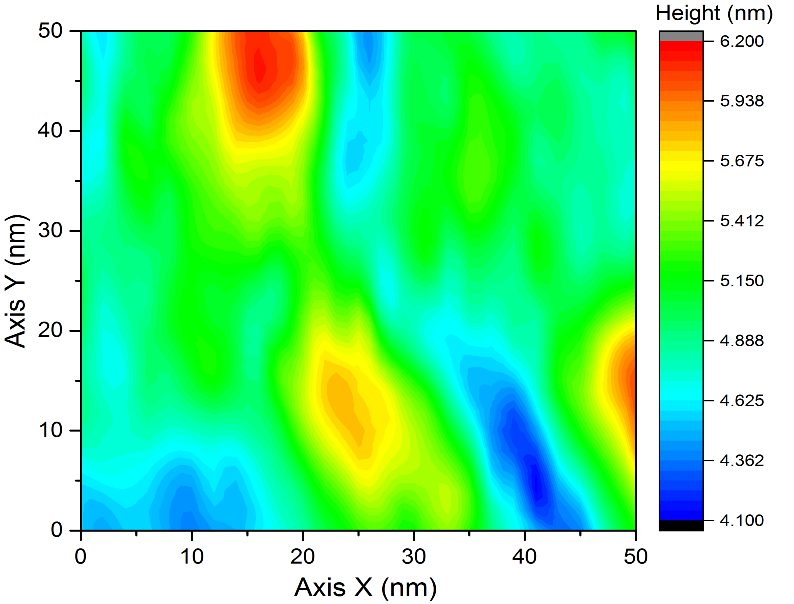
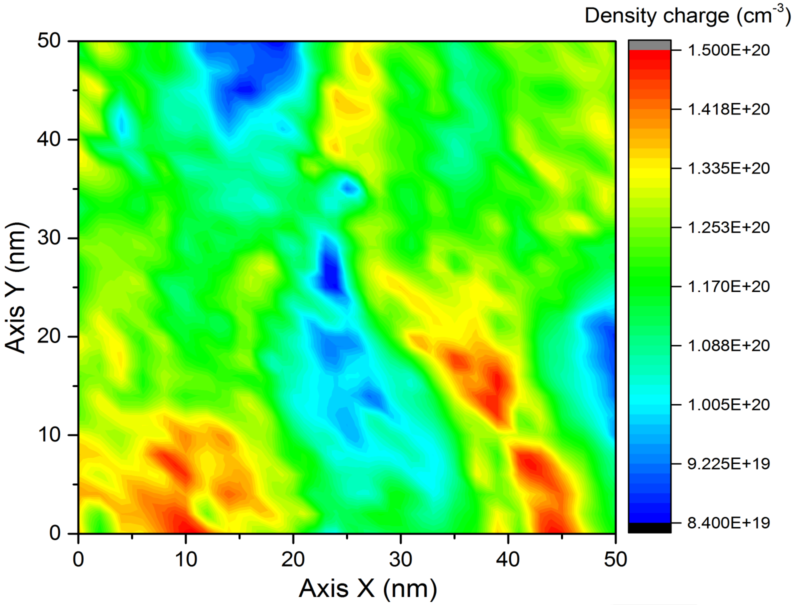
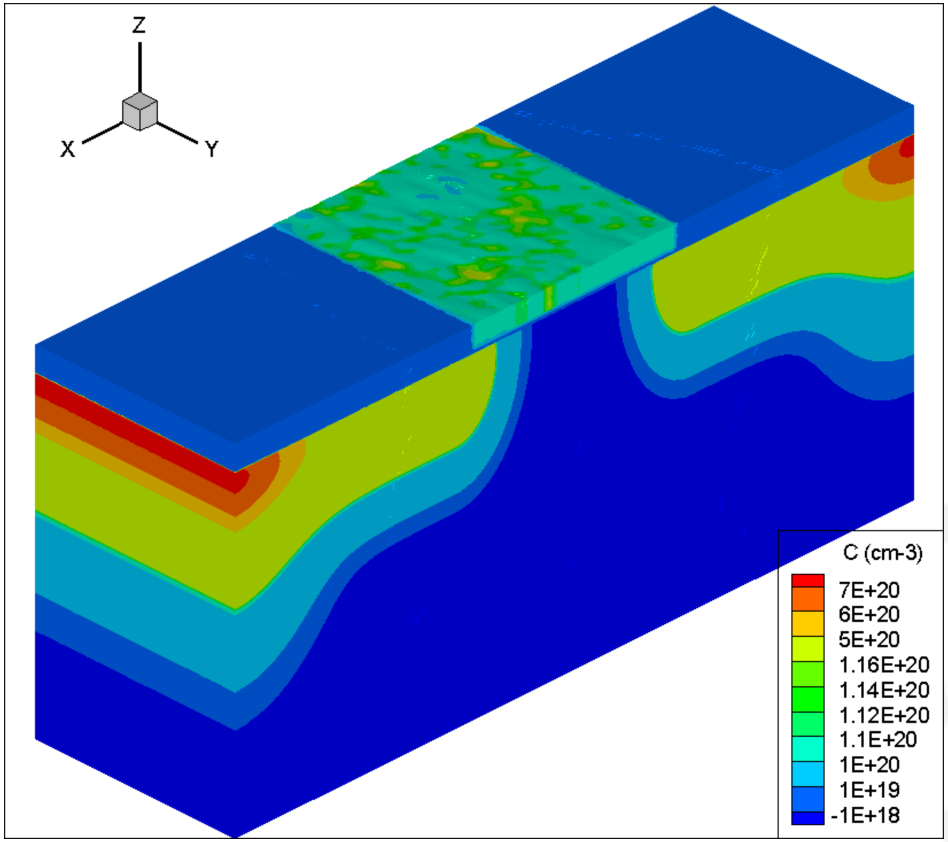




CiTIUS

Defects in high-k dielectrics

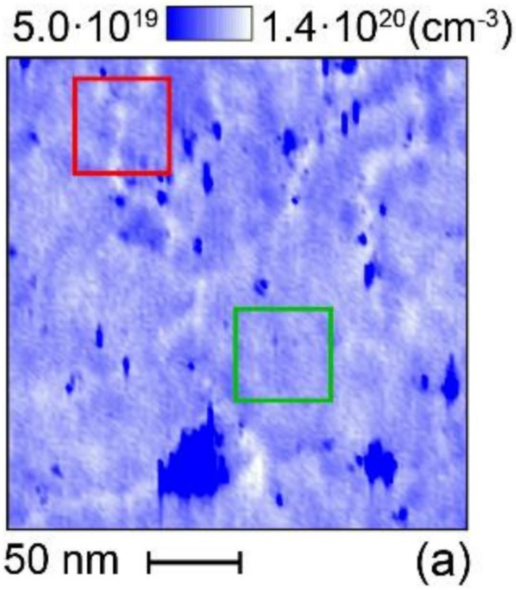
Modelling



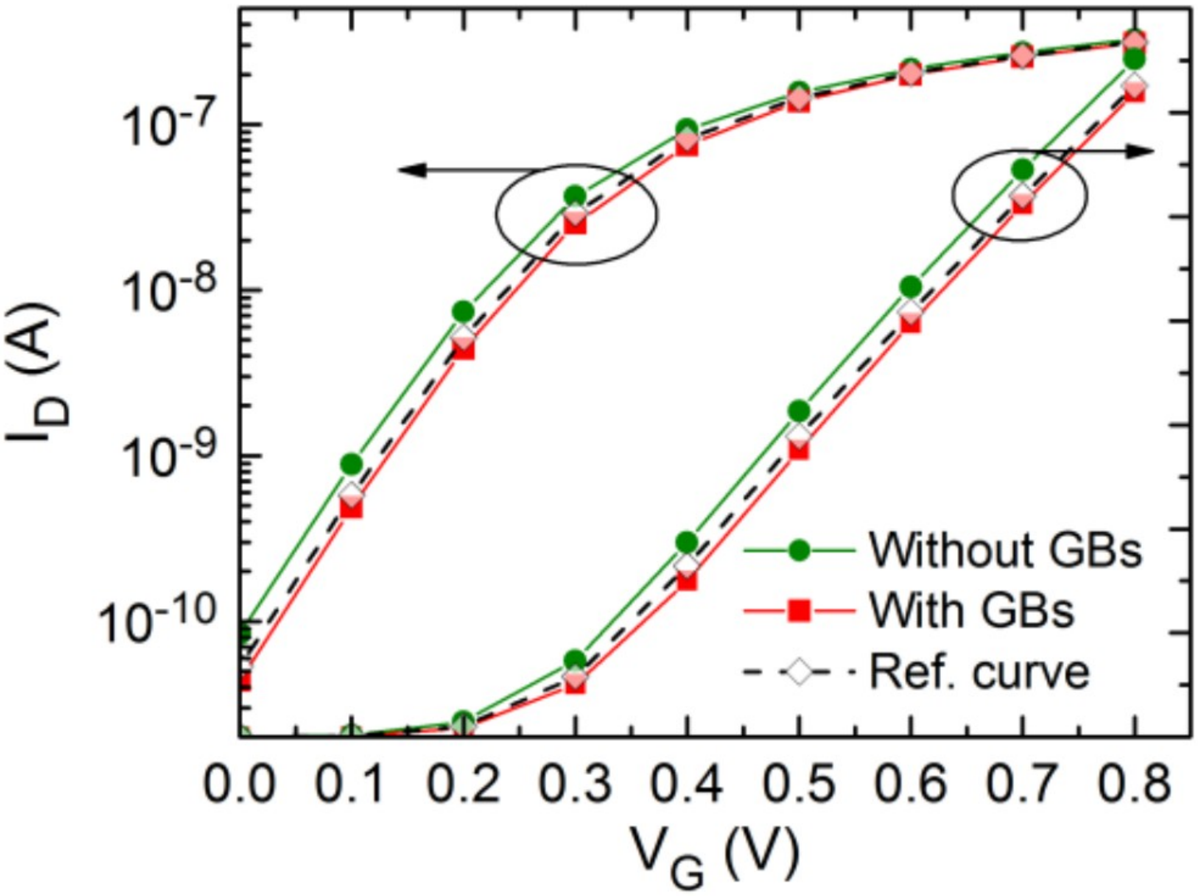
Si MOSFET device with a 50 nm gate length

Defects in high-k dielectrics

Modelling

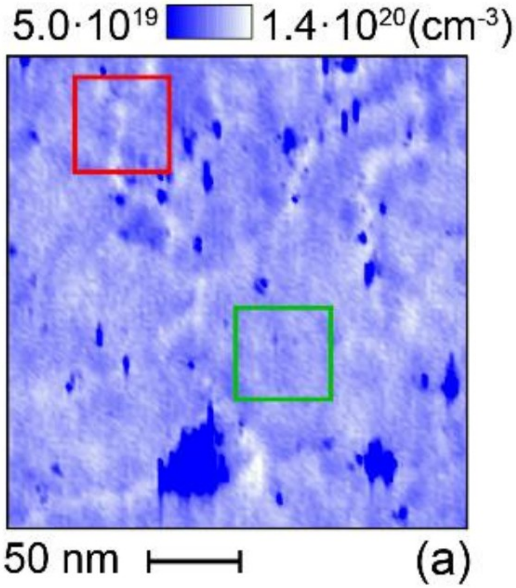


Experimental charge density map

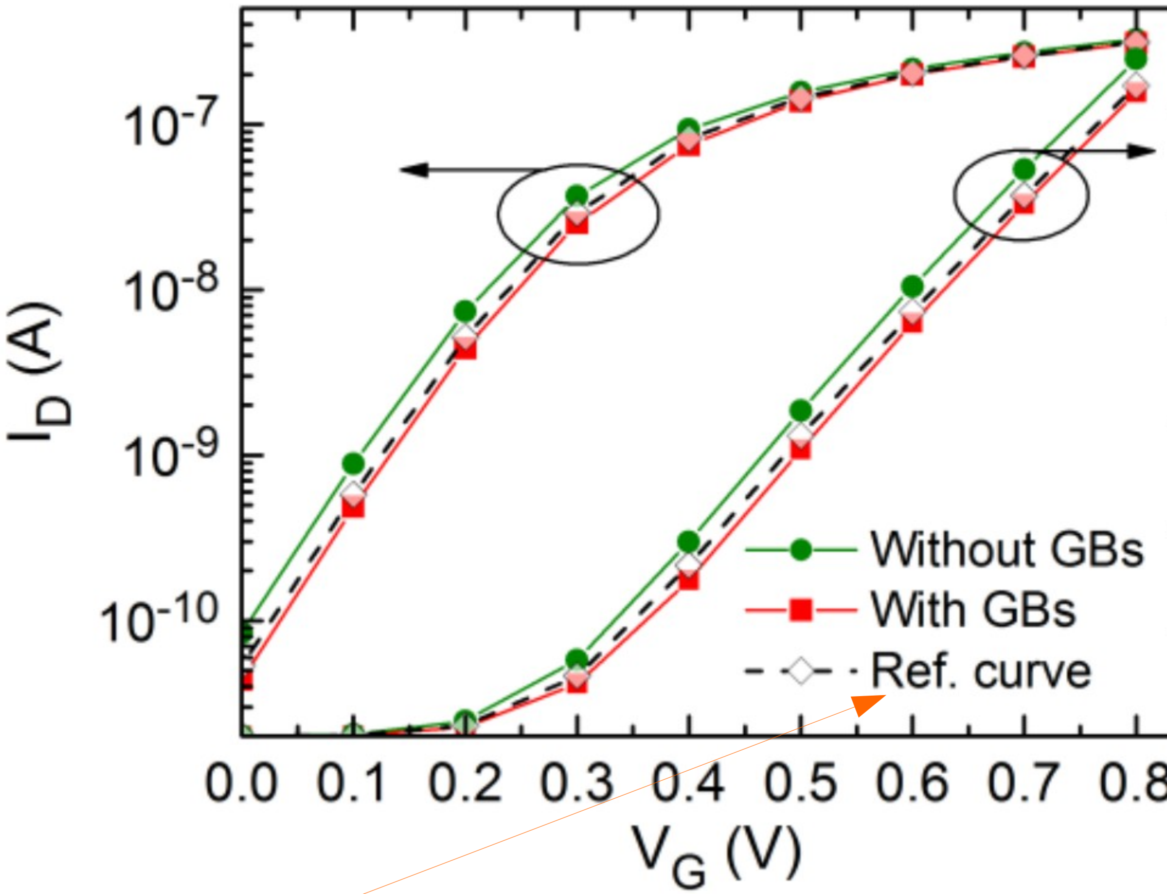


Defects in high-k dielectrics

Modelling



Experimental charge density map



Ref.= uniform HfO_2 thickness (5.3 nm) and trapped charge density ($10^{20}cm^{-3}$)

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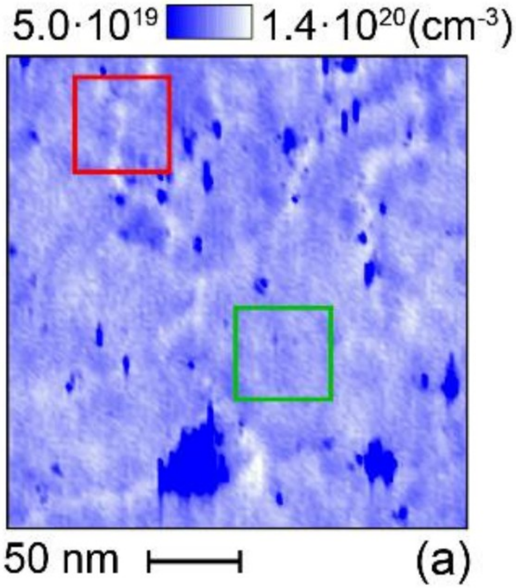
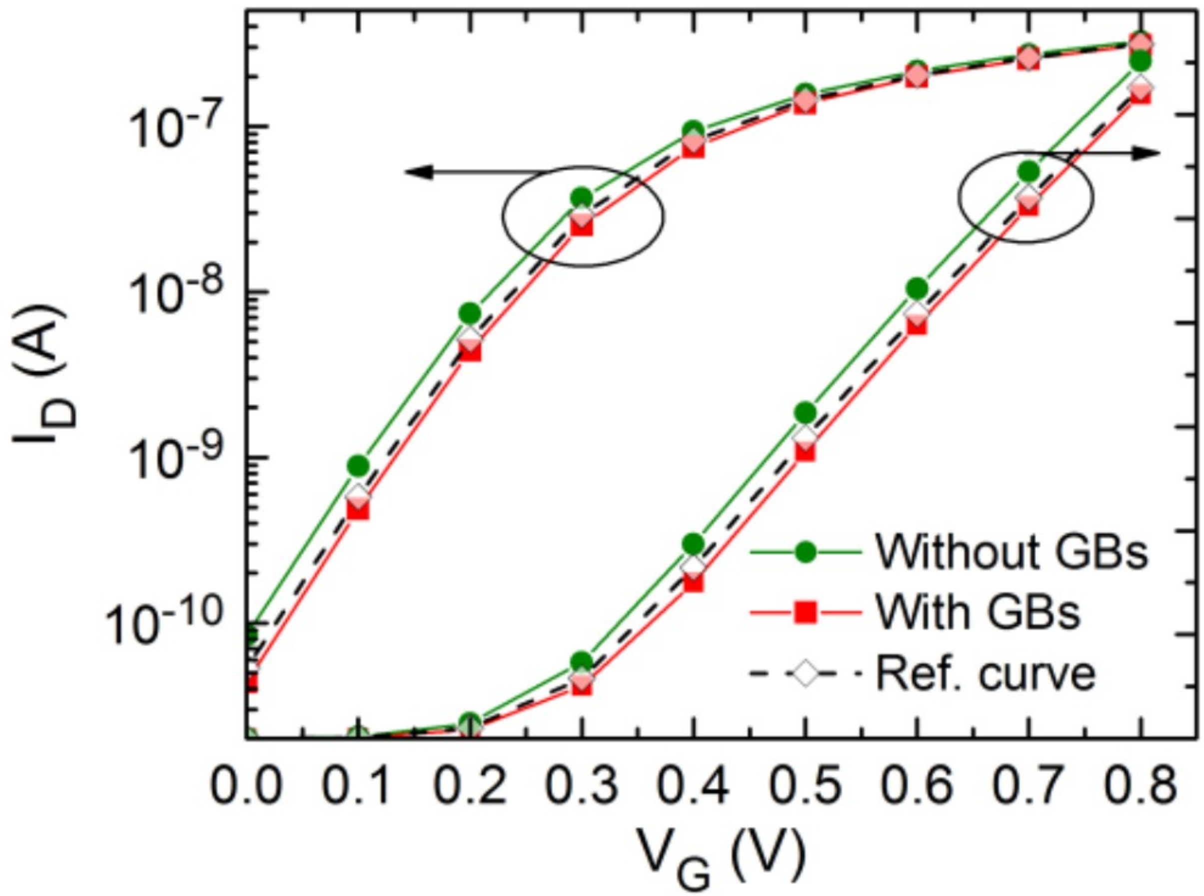
Defects in high-k dielectrics

Modelling



Experimental charge density map



Difference of 29.3 mV between the threshold voltages of the two simulated cases

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Variability sources

- Line edge roughness (LER)
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

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Variability sources

- Line edge roughness (LER)
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

Which is the dominant source of variability?
How do they compare?

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Variability sources

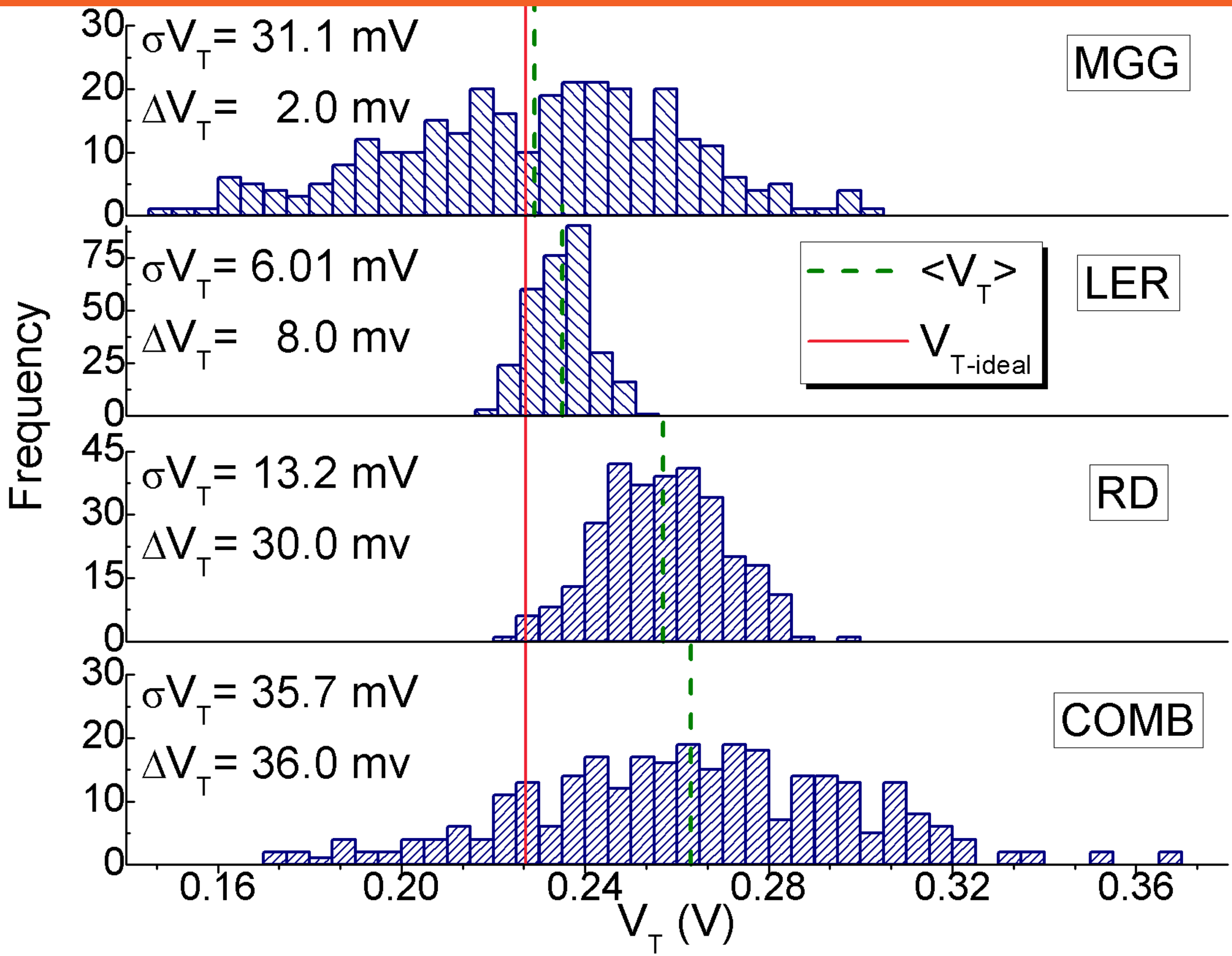
- Line edge roughness (LER)
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

Preliminar data
Results not available for FinFETs or nanowires yet

Which is the dominant source of variability?
How do they compare?

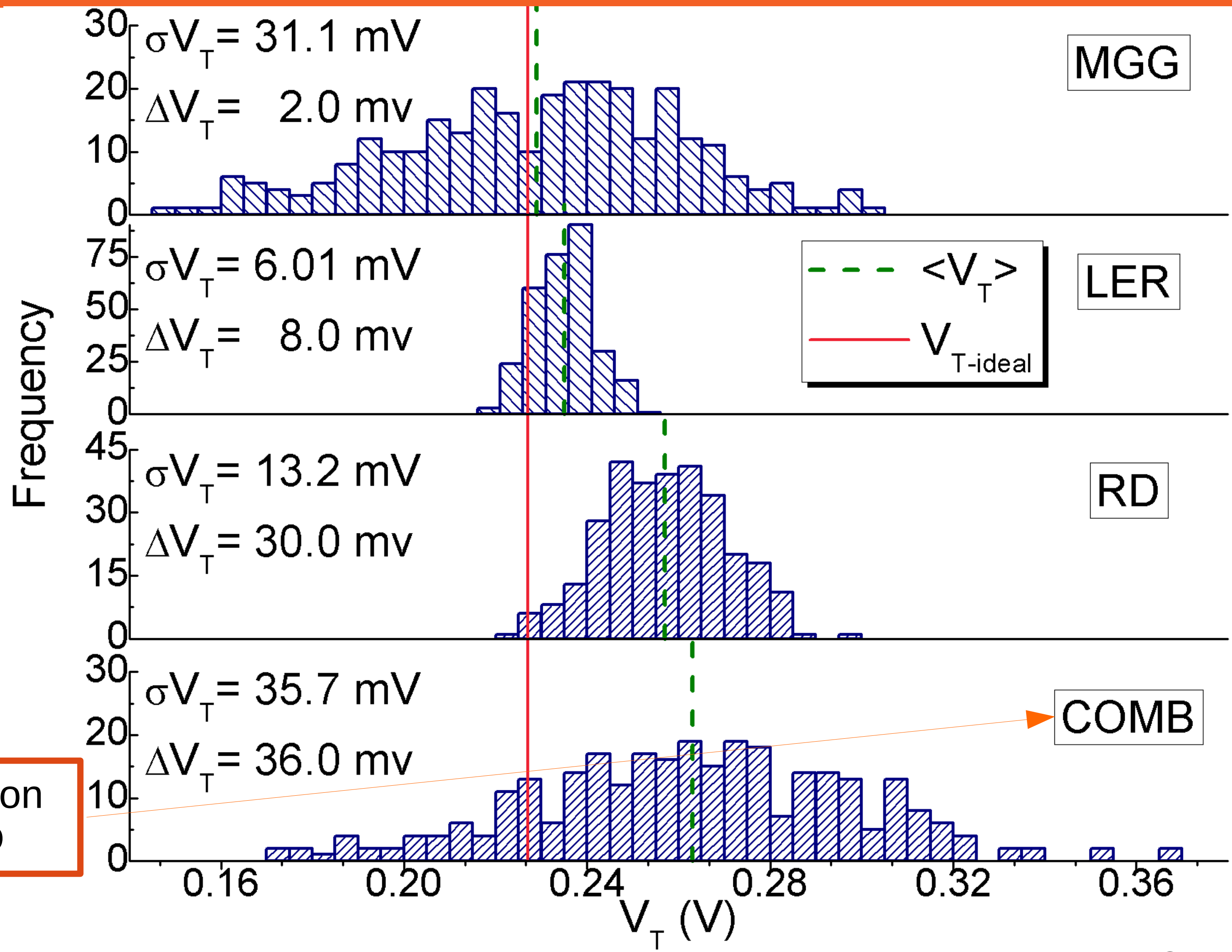
Comparison of variability sources

Histograms showing the V_T



Comparison of variability sources

Histograms showing the V_T

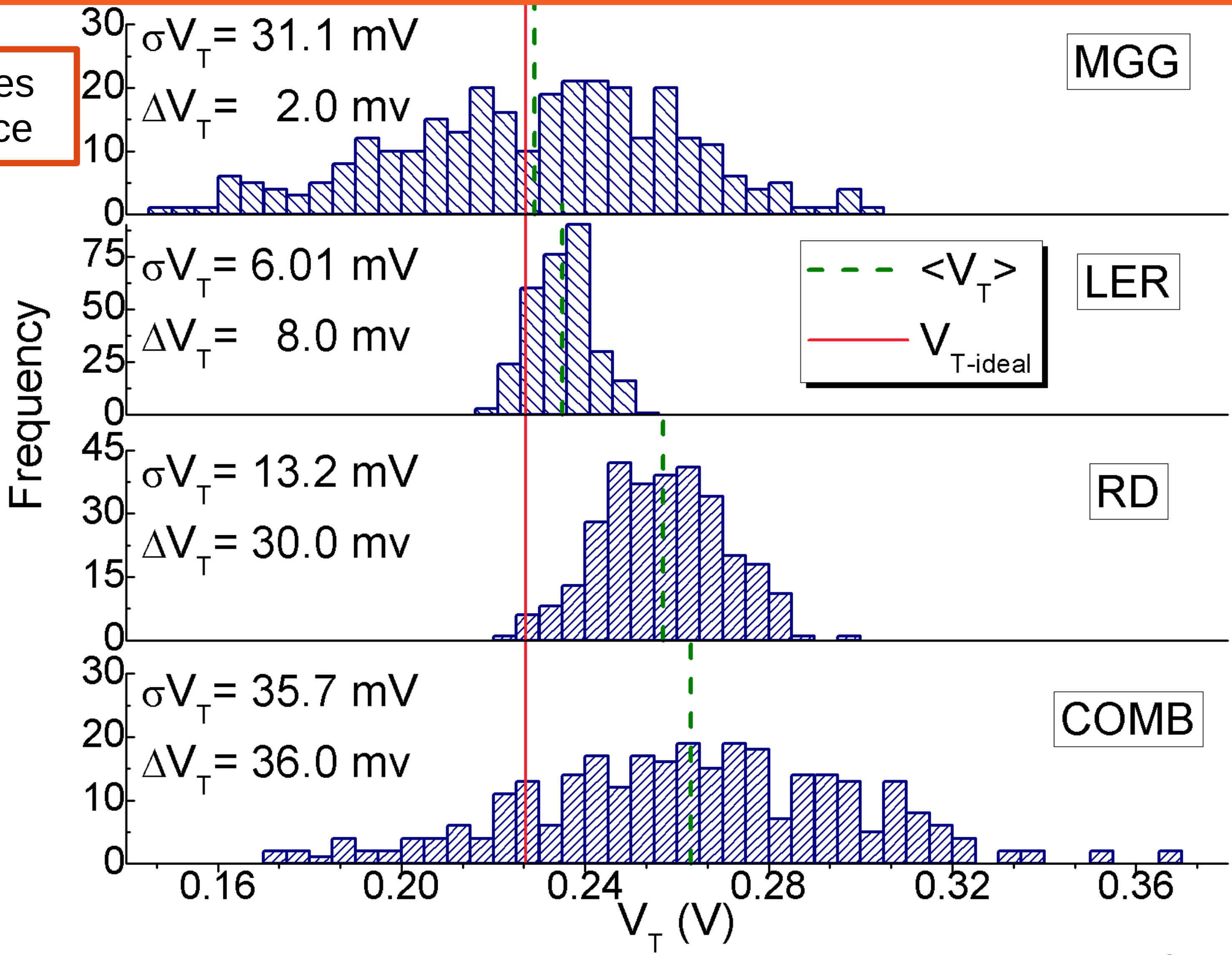


Combined simulation of MGG+LER+RD

Comparison of variability sources

Histograms showing the V_T

300 different devices per variability source

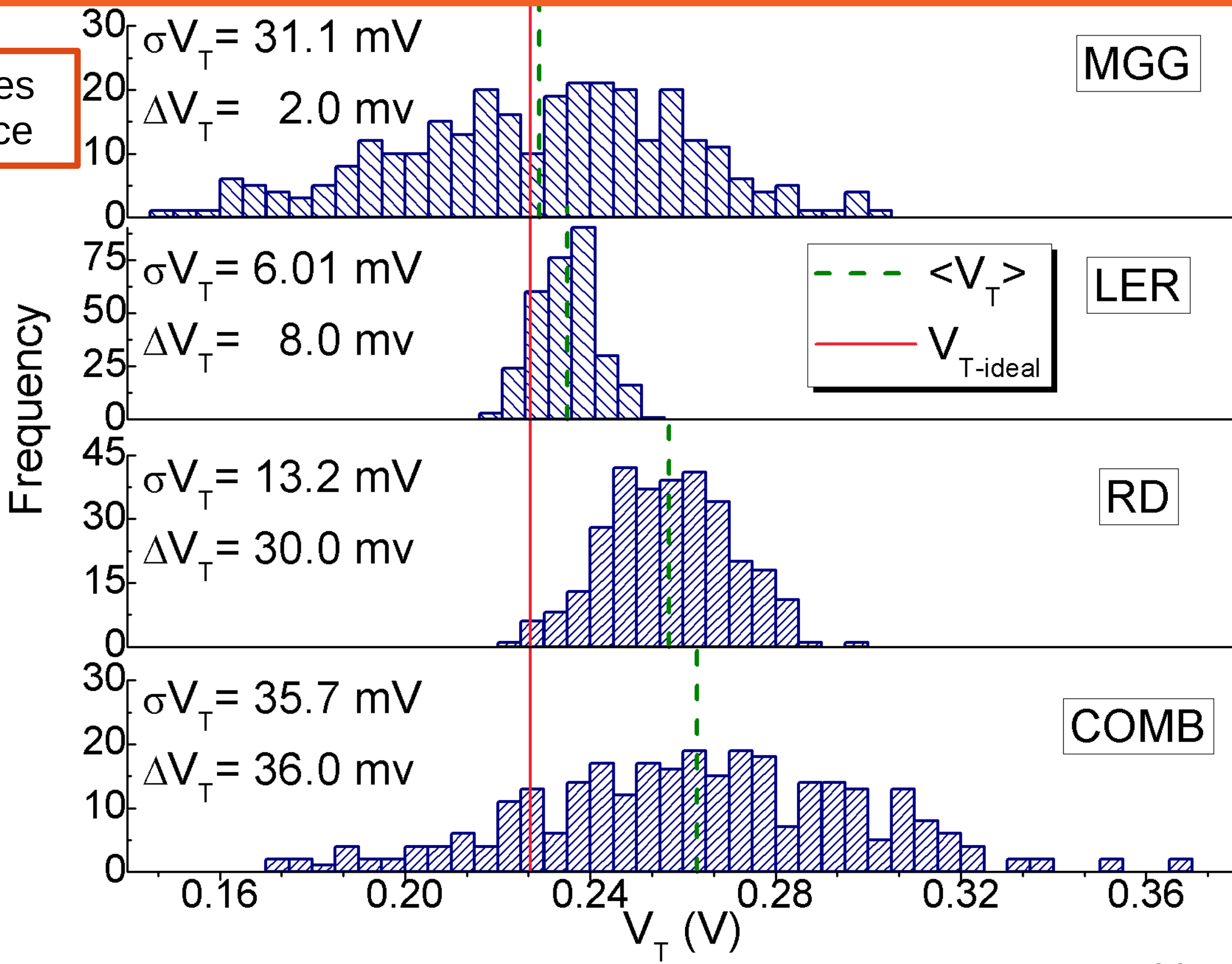


Comparison of variability sources

Histograms showing the V_T

300 different devices per variability source

10.4 nm gate length InGaAs FinFET



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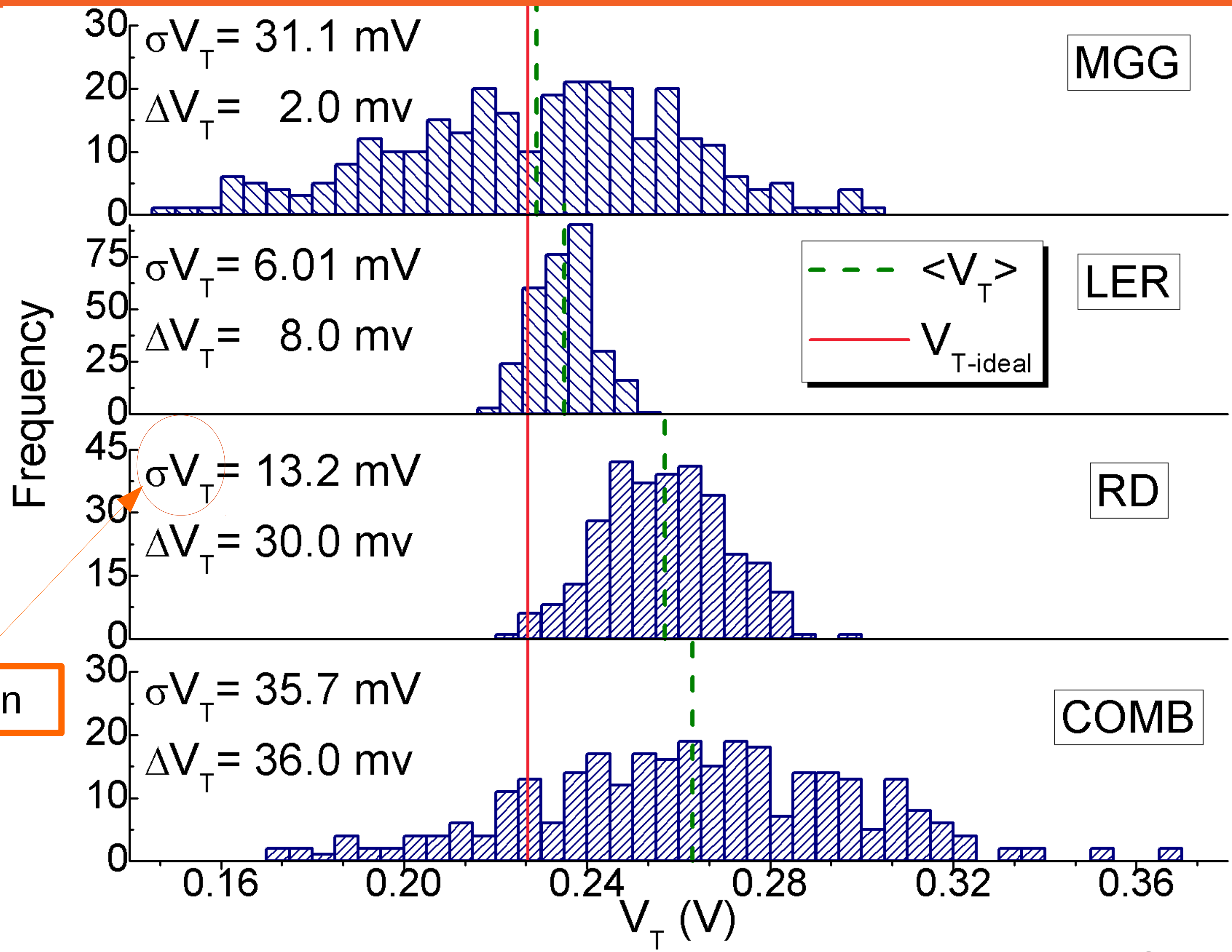
Comparison of variability sources

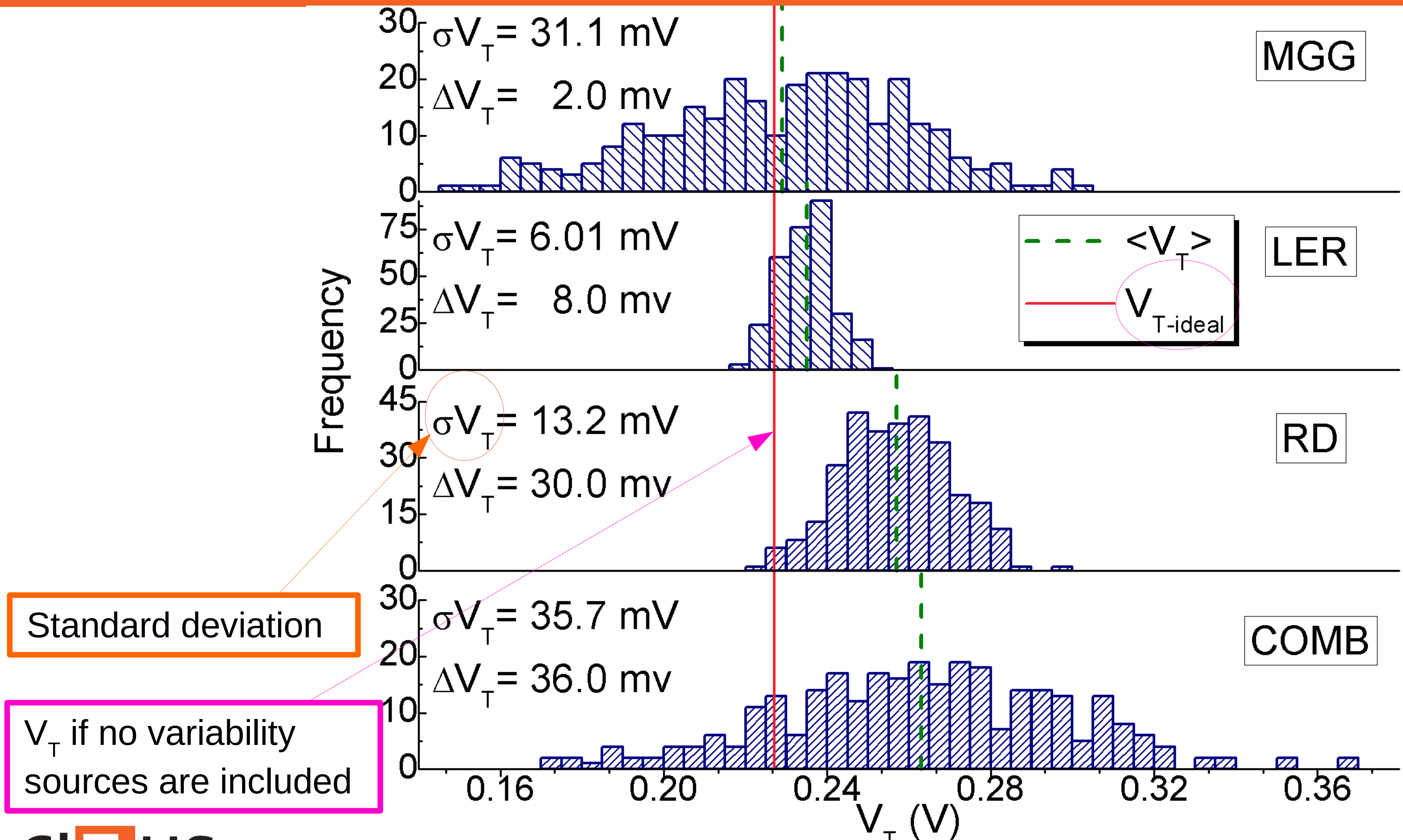
Histograms showing the V_T



Standard deviation

Comparison of variability sources

Histograms showing the V_T



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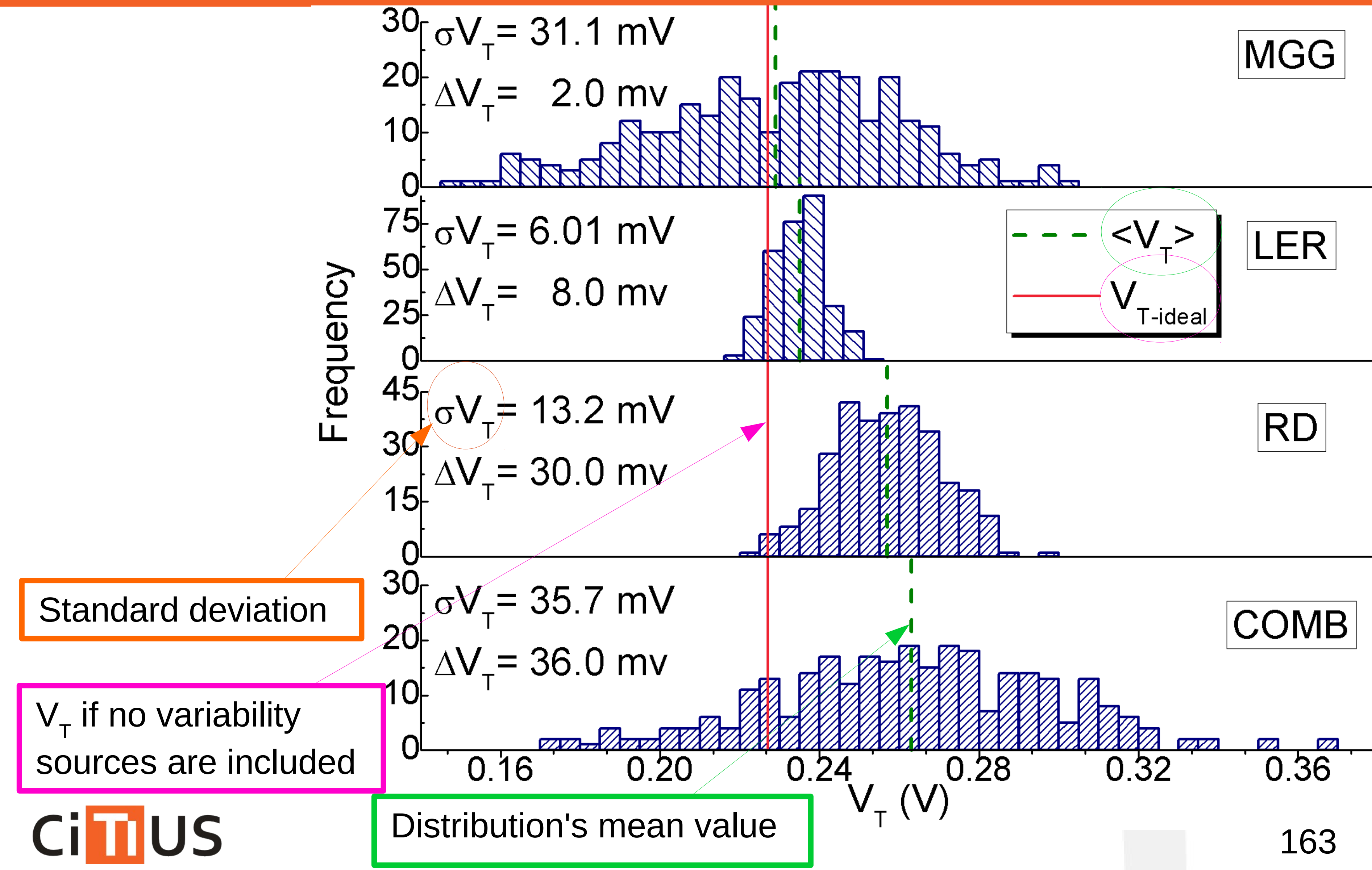
Comparison of variability sources

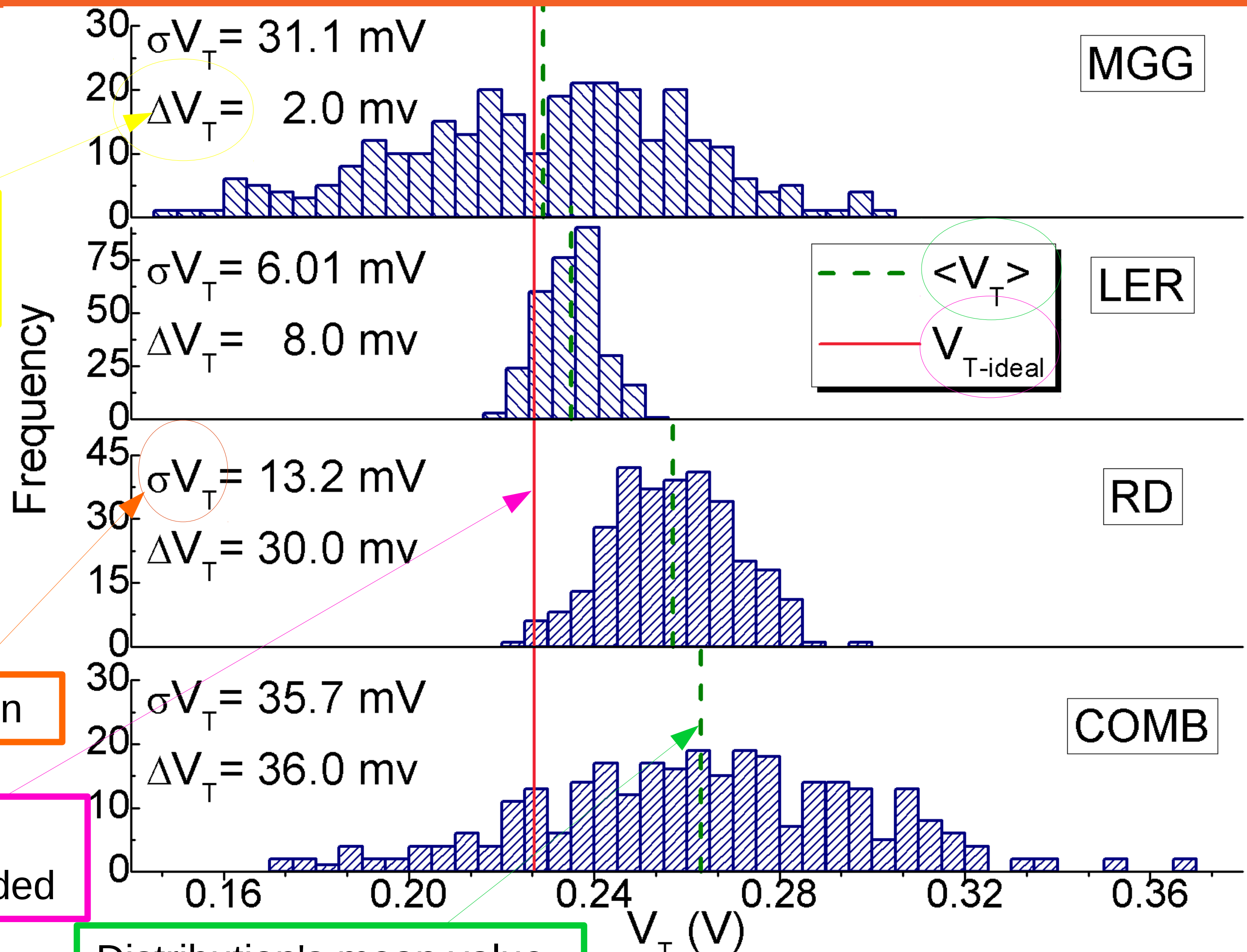
Histograms showing the V_T



CiTIUS

Comparison of variability sources

Histograms showing the V_T



V_T shift $=\langle V_T\rangle - V_{T\text{-ideal}}$

Standard deviation

V_T if no variability sources are included

Distribution's mean value

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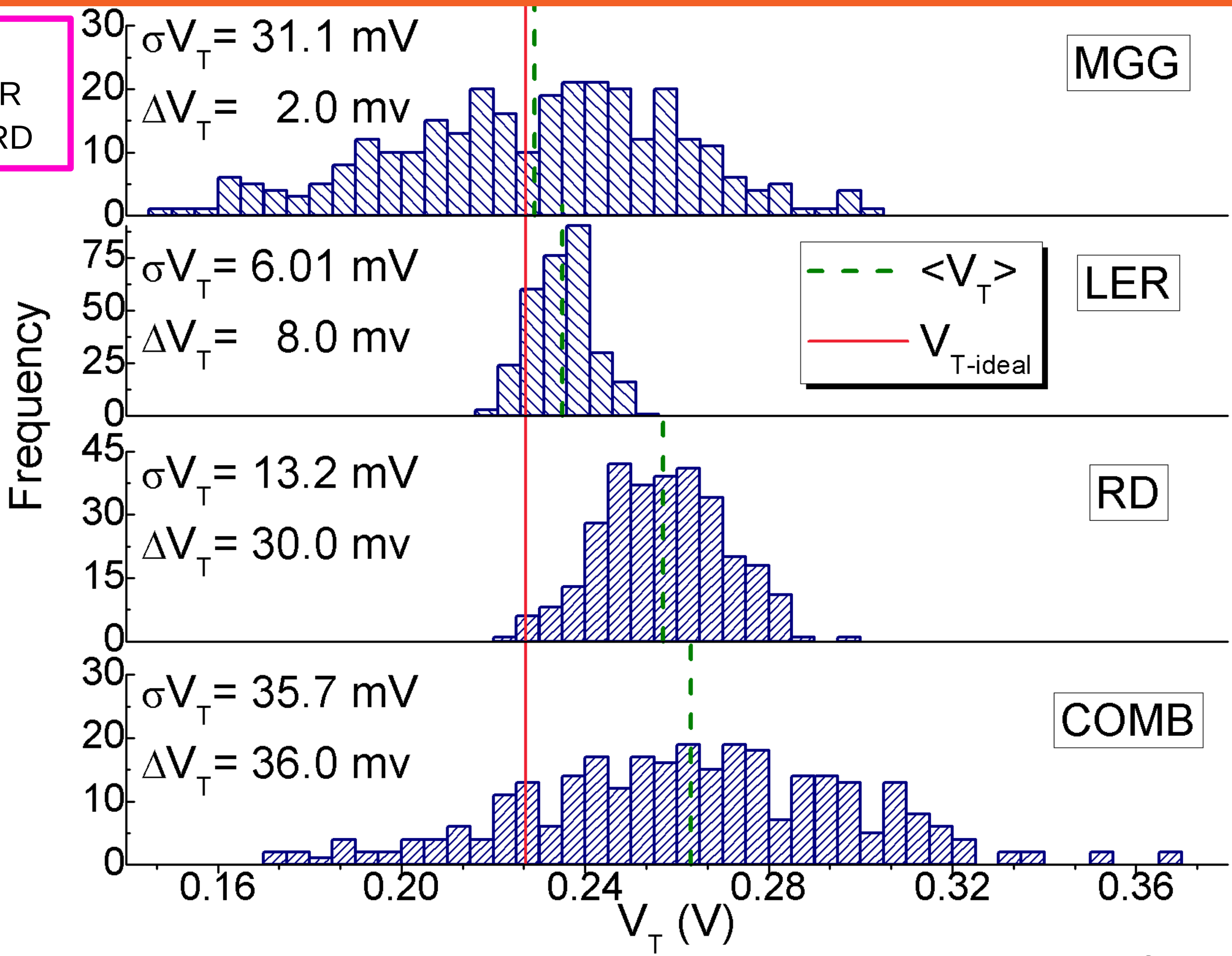
Comparison of variability sources

Histograms showing the V_T

MGG dominant

5 times larger than LER

2.3 times larger than RD



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Comparison of variability sources

Histograms showing the V_T

MGG dominant

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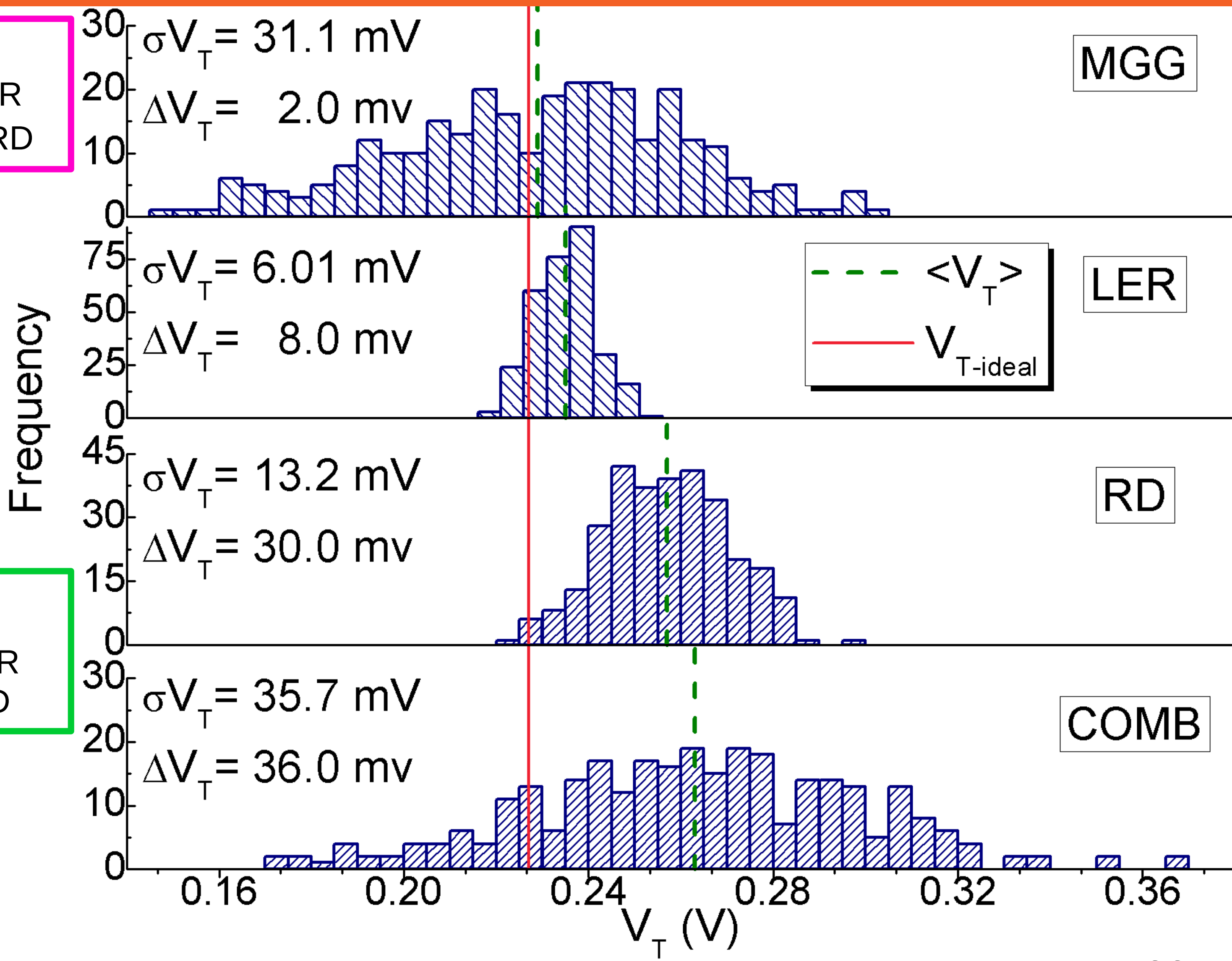


MGG ΔV_T minimal

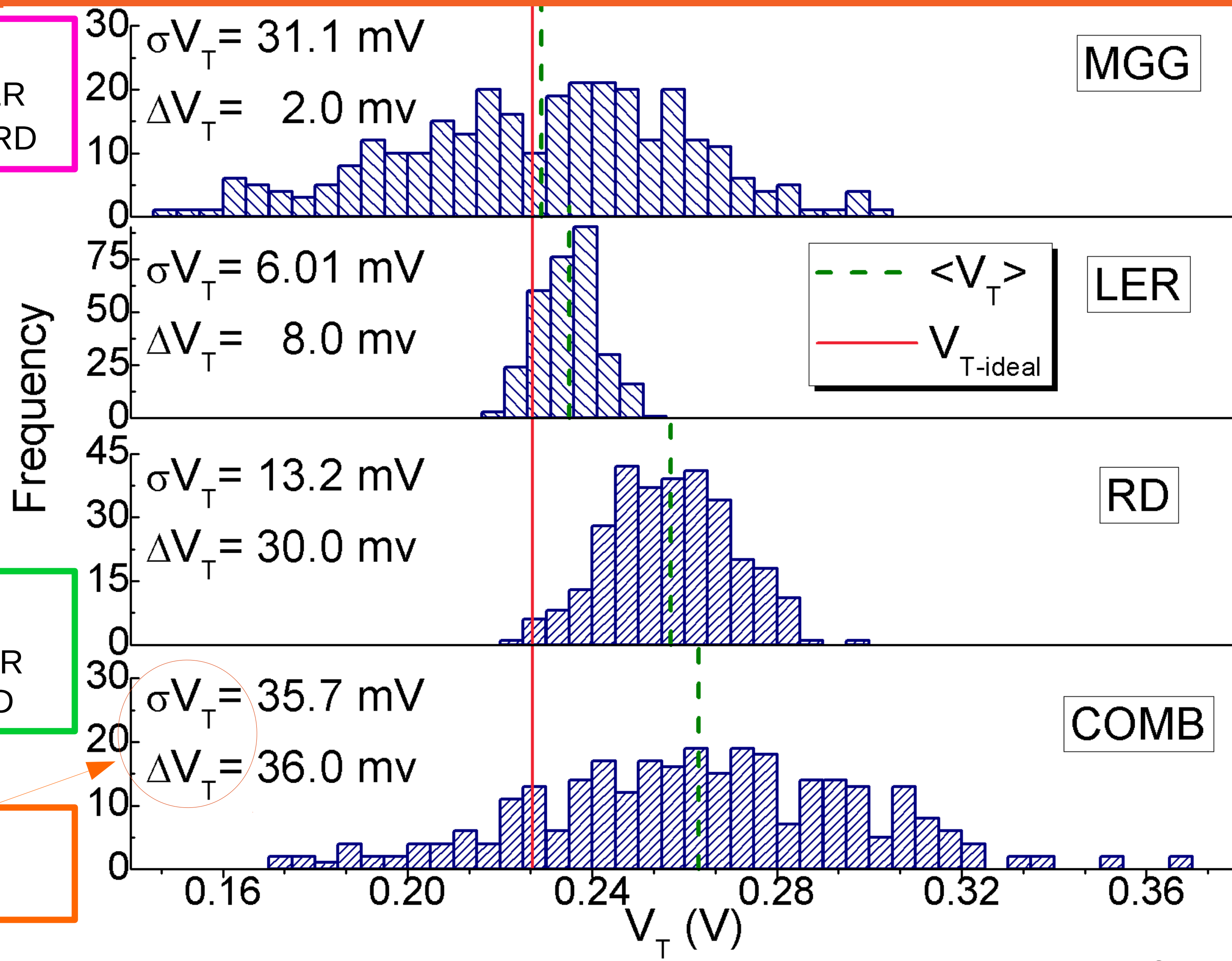
4 times lower than LER

15 times lower than RD

Comparison of variability sources

Histograms showing the V_T

MGG dominant
5 times larger than LER
2.3 times larger than RD



MGG ΔV_T minimal
4 times lower than LER
15 times lower than RD

A more realistic scenario

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Variability sources

- Line edge roughness (LER)
- Metal grain granularity (MGG)
- Random dopants (RD)
- Defects in high-k dielectrics

Which is the dominant source of variability?
How do they compare?

What is the computational cost?

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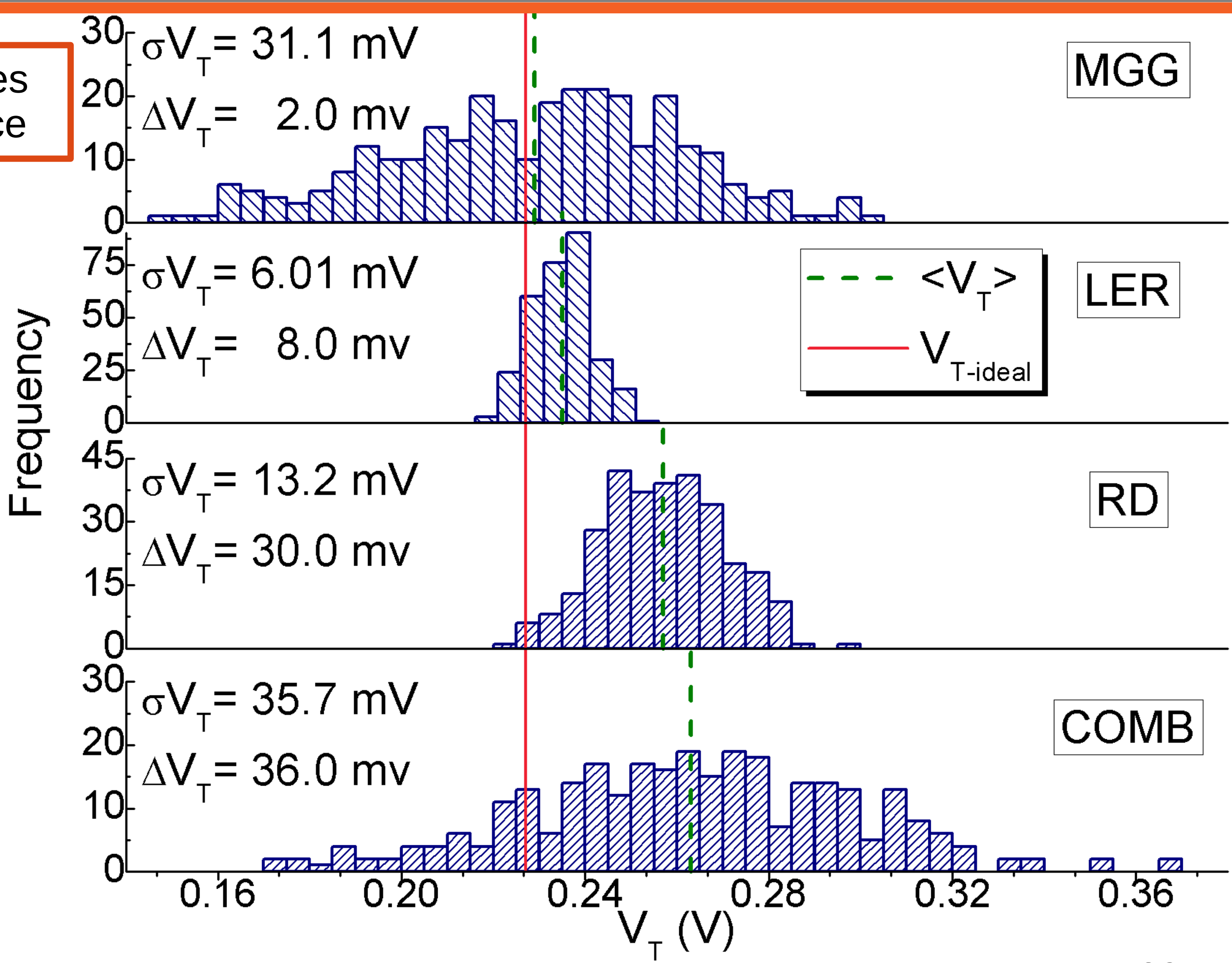
Computational cost

Cluster attack!!

300 different devices
per variability source



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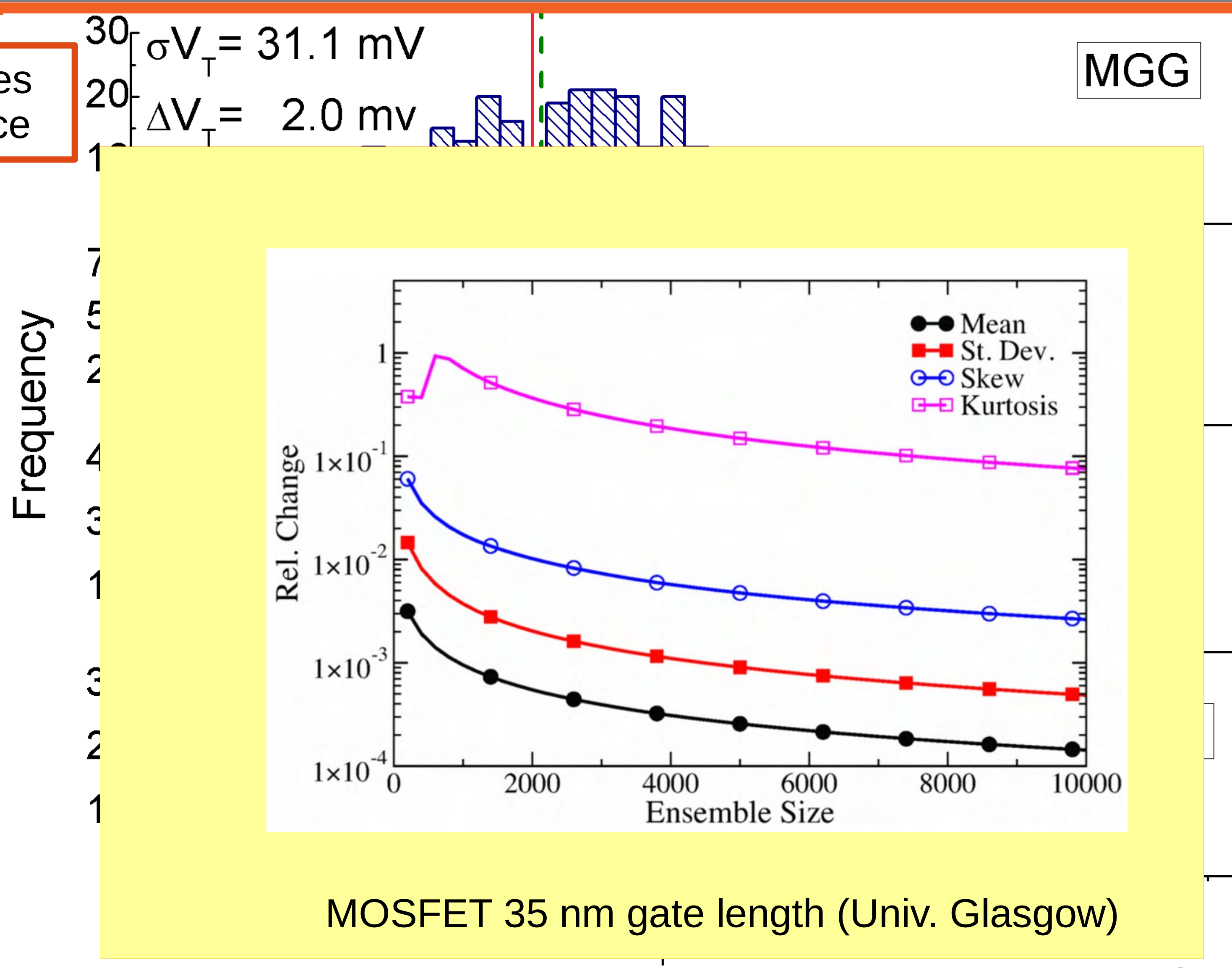
Computational cost

Cluster attack!!

300 different devices per variability source



MOSFET 35 nm gate length (Univ. Glasgow)

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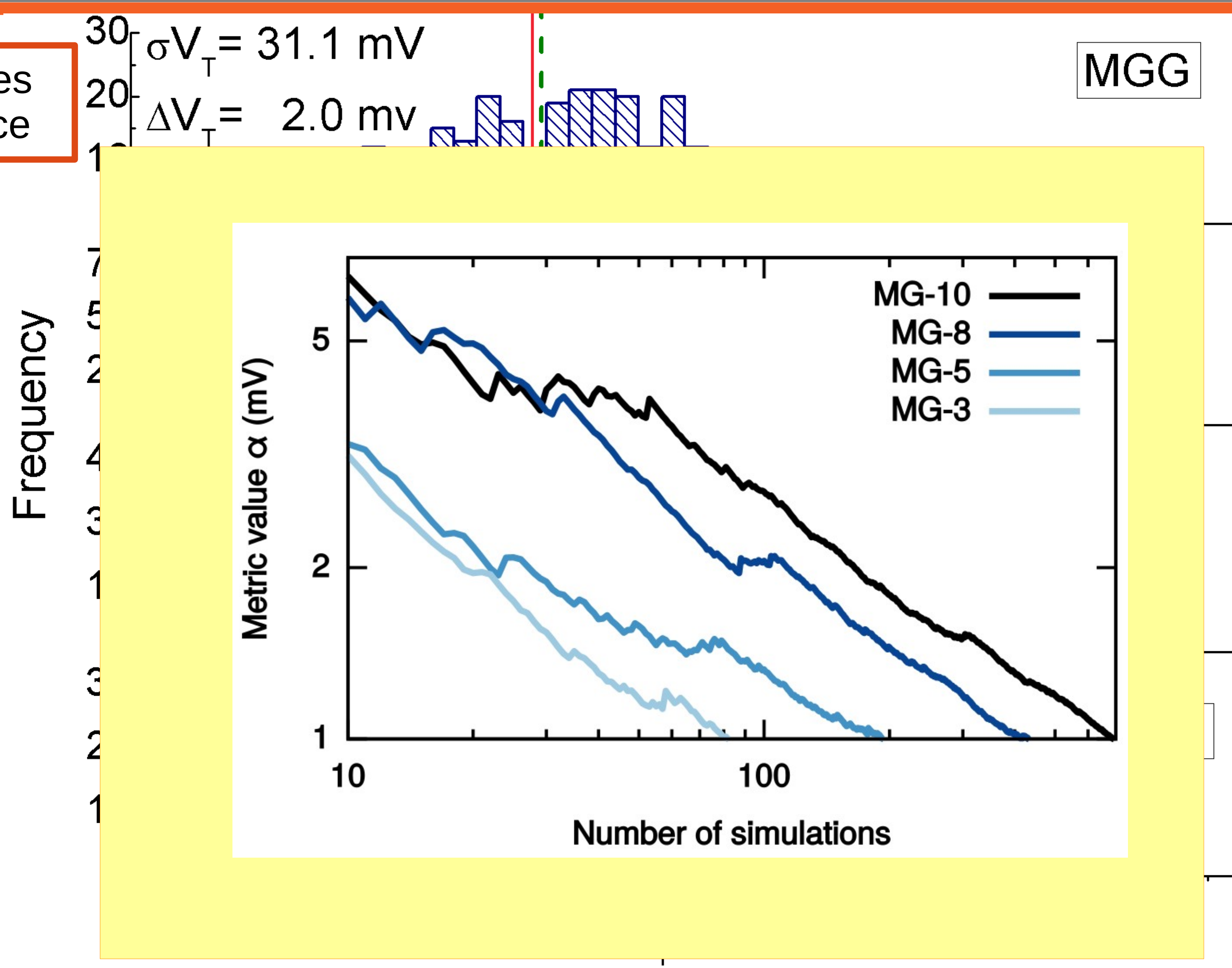
Computational cost

Cluster attack!!

300 different devices per variability source



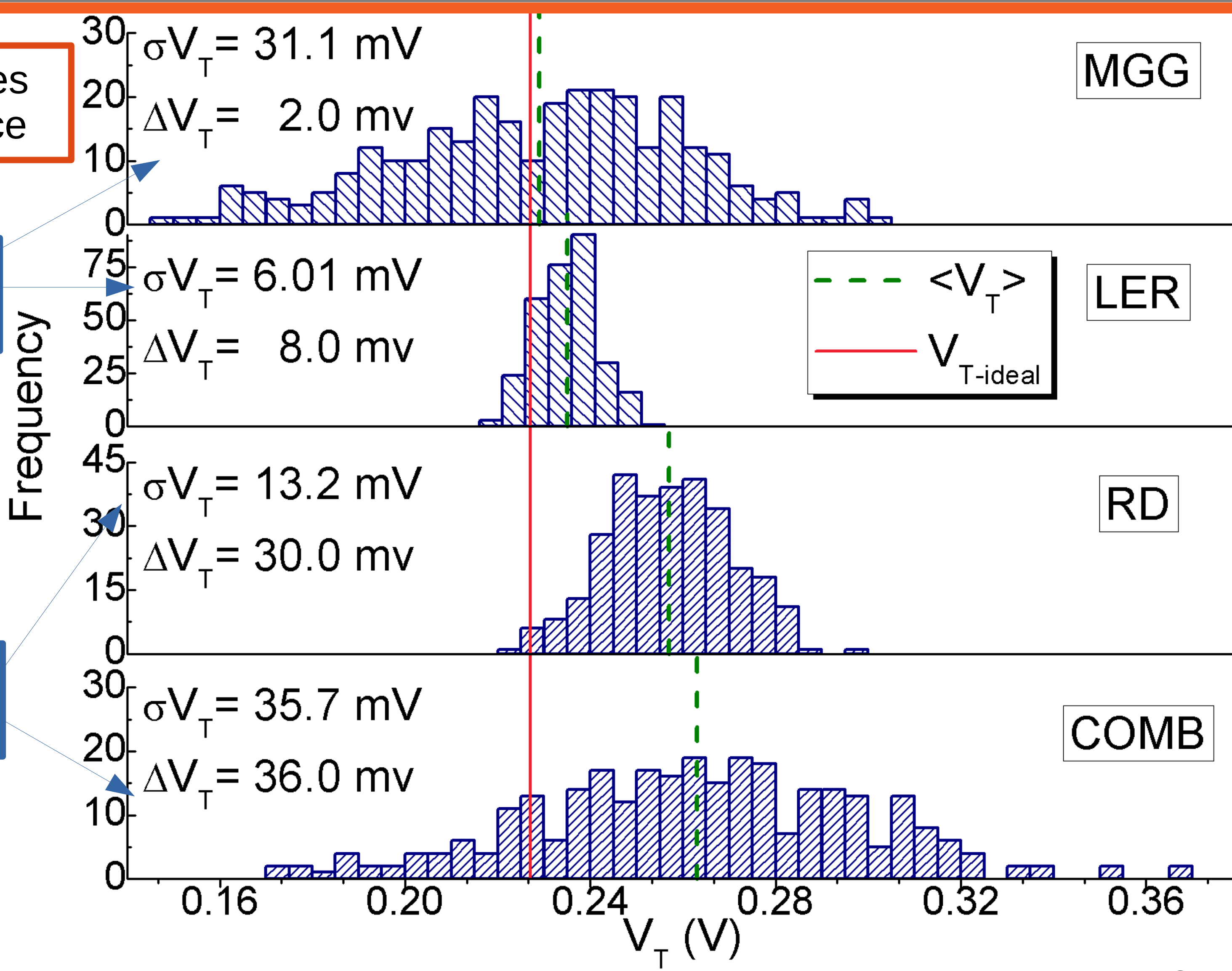
Computational cost

Cluster attack!!

300 different devices per variability source

24 hr/sim 1 core (cluster ctcomp2)

36 hr/sim 1 core (cluster ctcomp2)



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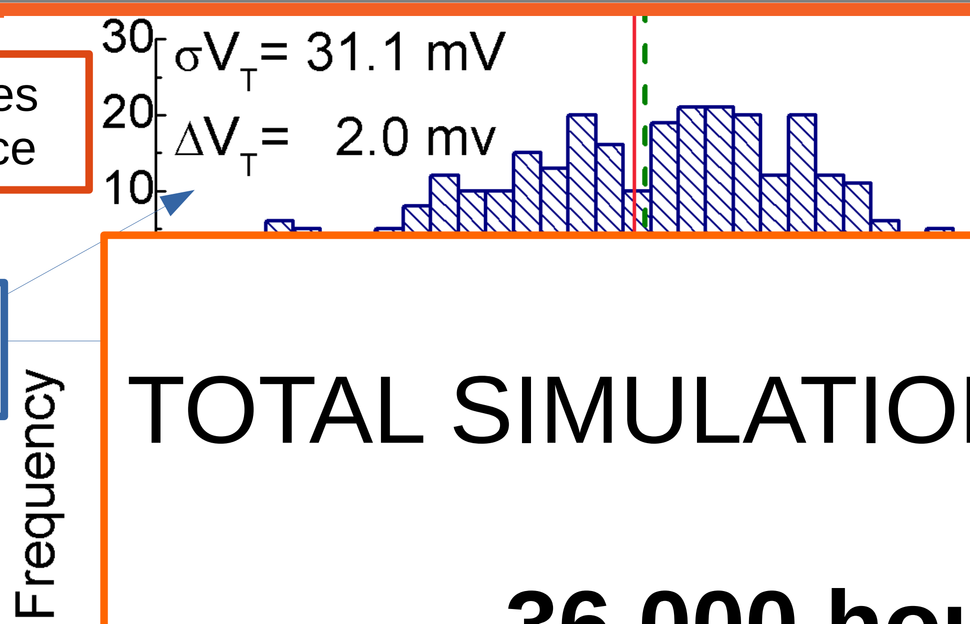
Computational cost

Cluster attack!!

300 different devices per variability source



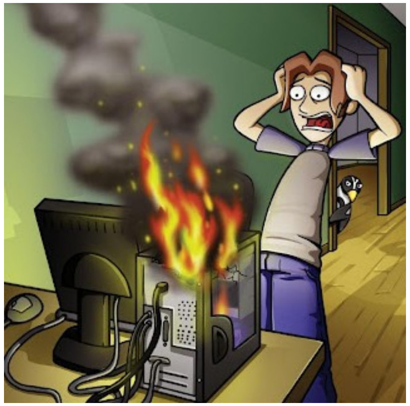
24 hr/sim 1 core (cluster ctcomp2)

36 hr/sim 1 core (cluster ctcomp2)

TOTAL SIMULATION TIME:

36,000 hours

Conservative estimation !!



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Numerical results

- Why do we care about variability?
- Variability pipeline
- Variability sources
- **How can we know more?**

One of the main burdens of a TCAD **variability** study of semiconductor devices is its **high computational cost**.

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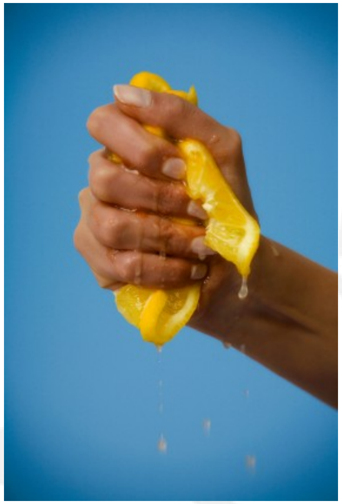

How can we know more?

Motivation

One of the main burdens of a TCAD **variability** study of semiconductor devices is its **high computational cost**.

We developed a **new approach**, based on the creation of **fluctuation sensitivity maps**, that provides:

1.- **spatial information** about the effect of the variability on the device performance

2.- a **prediction** of the magnitude of the variability

This technique allow us to obtain simulation results at a **reduced time**

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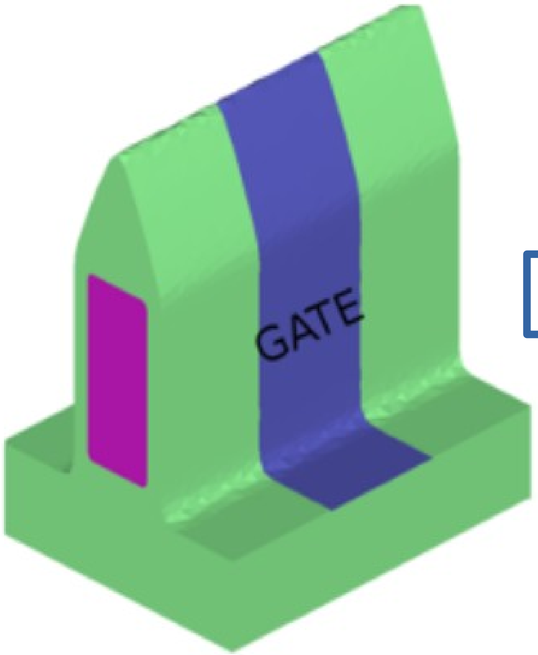
How can we know more?

Fluctuation Sensitivity Map (**FSM**)

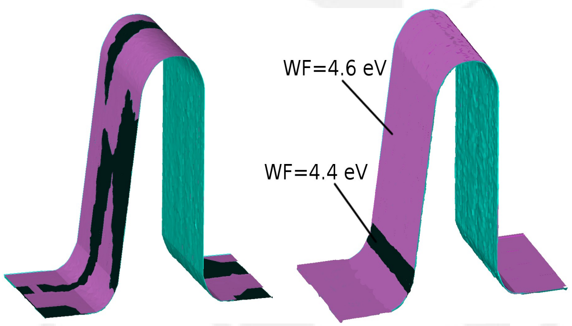


MGG variability

300 simulations

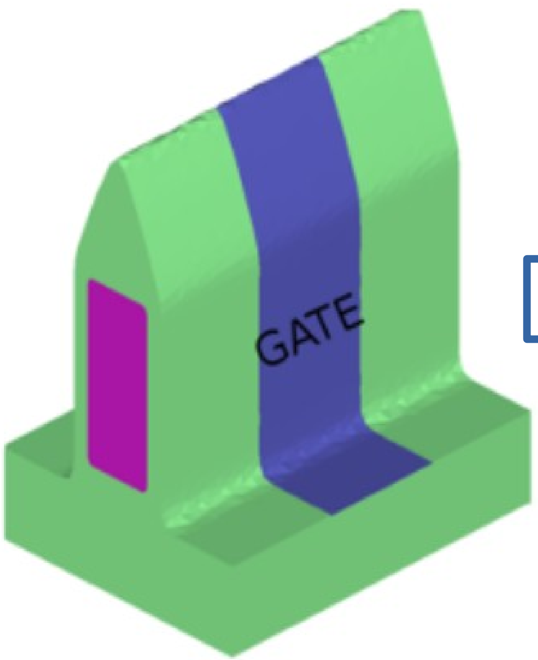
FoM values (V_T, I_{OFF}, I_{ON}, etc.)

Gate profiles



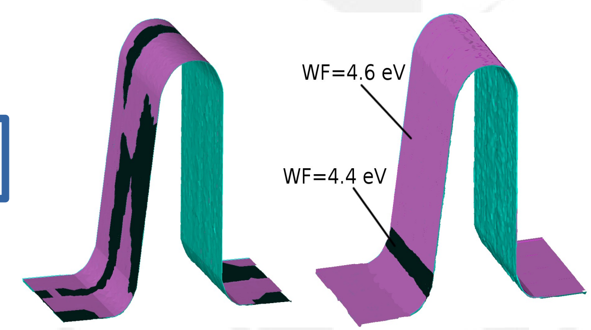
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



300 simulations → FoM values (V_T, I_{OFF}, I_{ON}, etc.)

300 simulations → Gate profiles



Objective:

→ obtain valuable **spatial information** about the effect of the MGG

→ useful in the development of **fluctuation-resistant** device architectures

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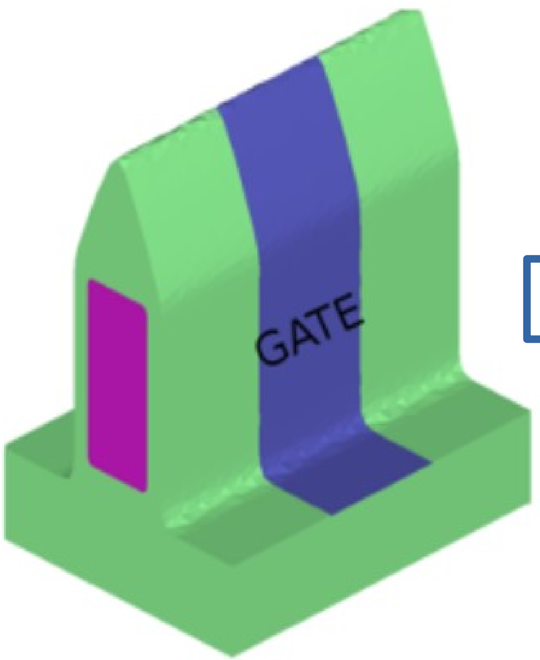
How can we know more?

Fluctuation Sensitivity Map (**FSM**)

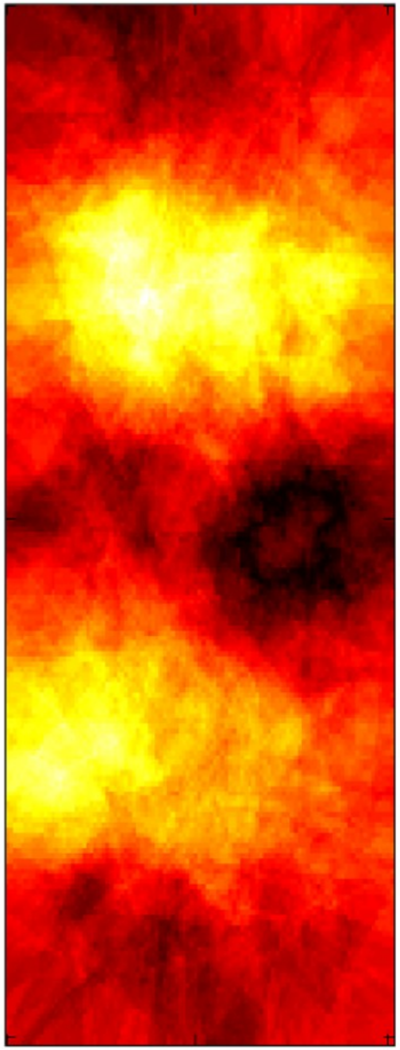


300 simulations

FoM values

Gate profiles

The value of an element $FSM_{i,j}$ represents how sensitive a certain figure of merit is to the grain orientation at the position in the gate.



Fluctuation Sensitivity Map

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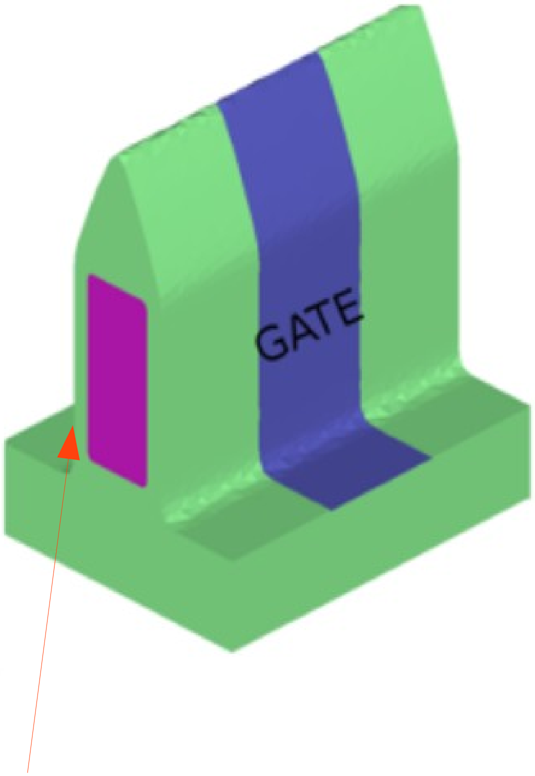
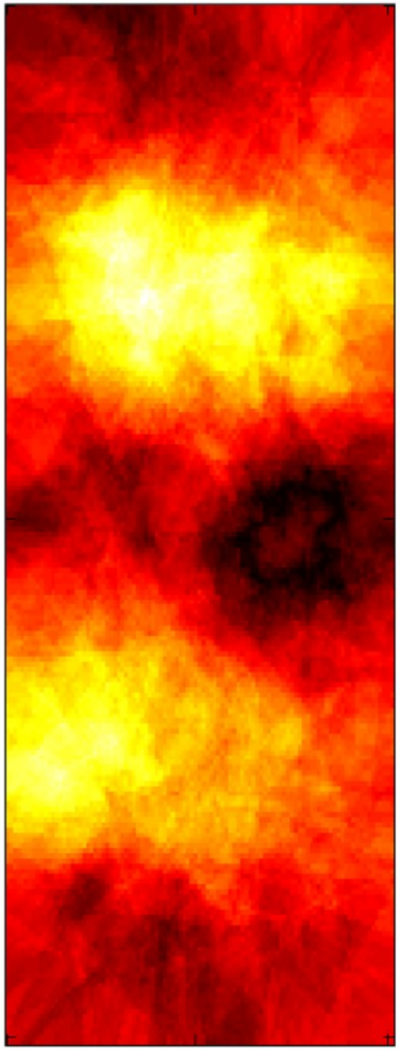
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



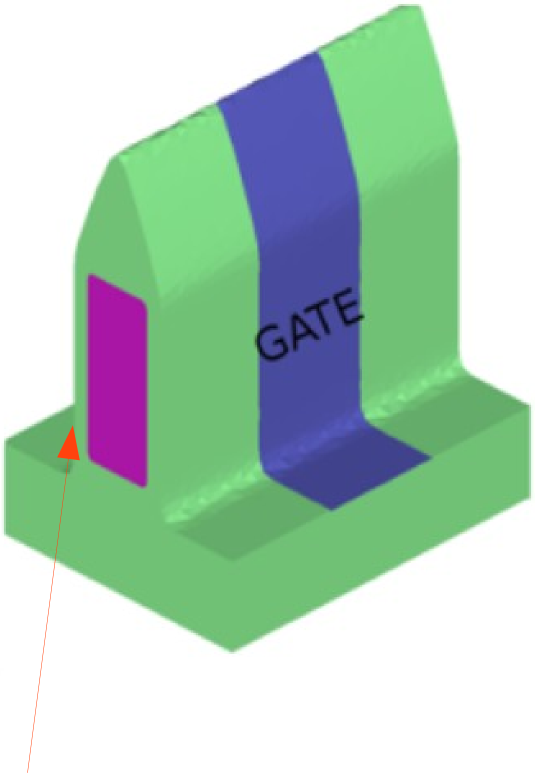
Bottom gate left



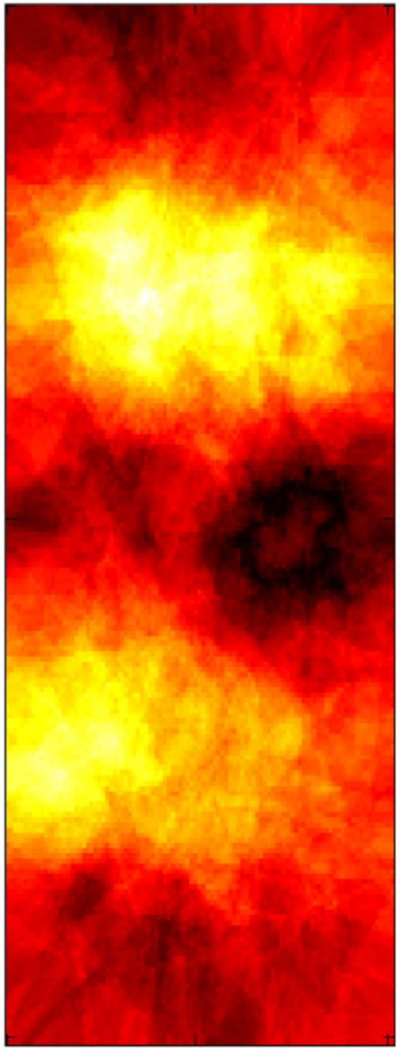
Fluctuation Sensitivity Map

How can we know more?

Fluctuation Sensitivity Map (**FSM**)



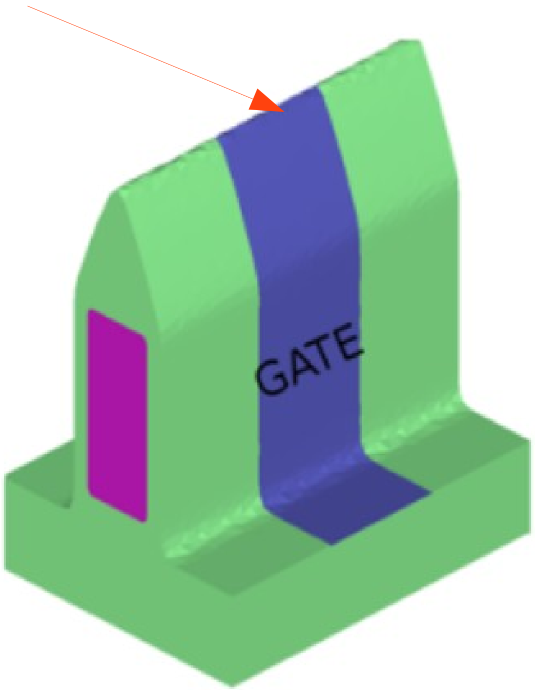
Bottom gate left



Fluctuation Sensitivity Map

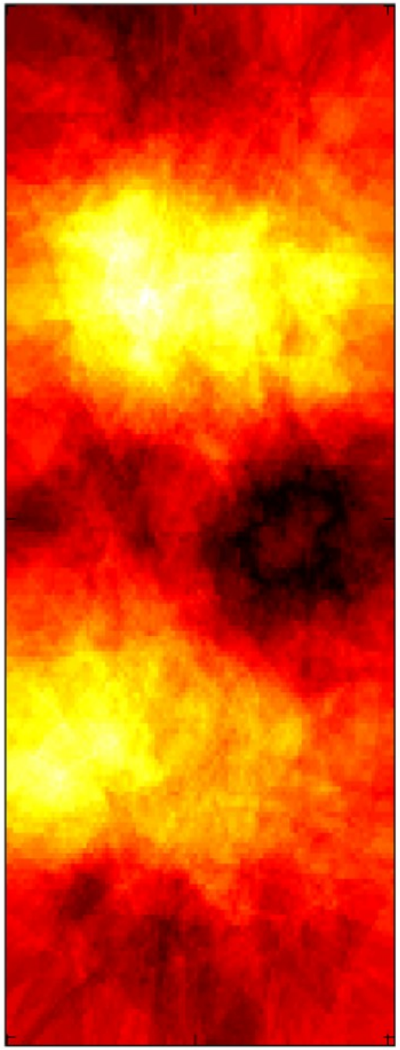
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



Bottom gate left

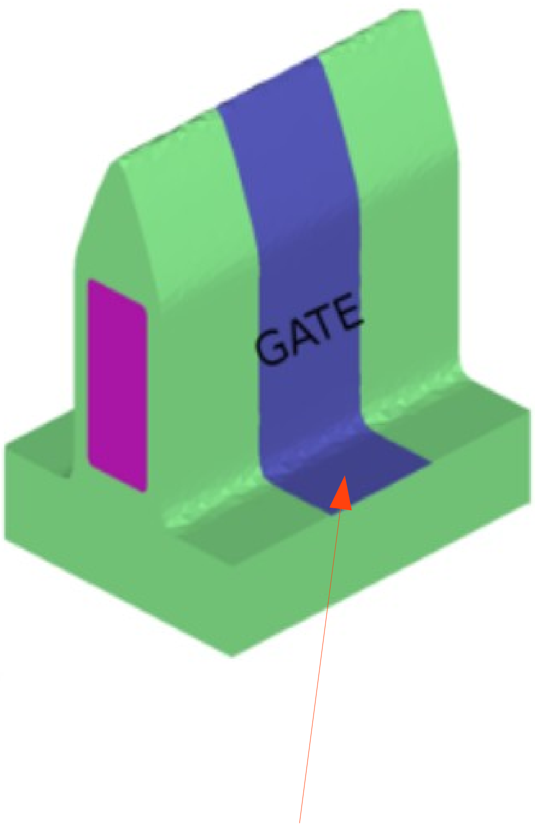
Top gate



Fluctuation Sensitivity Map

How can we know more?

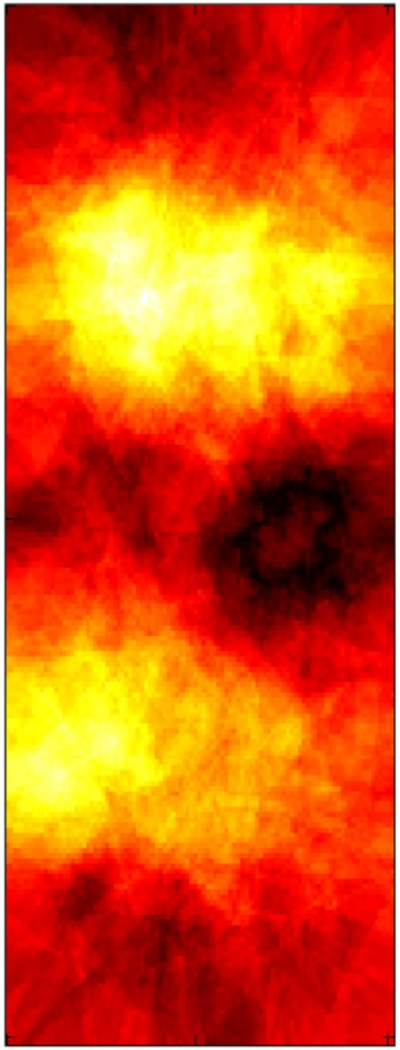
Fluctuation Sensitivity Map (**FSM**)



Bottom gate left

Top gate

Bottom gate right



Fluctuation Sensitivity Map

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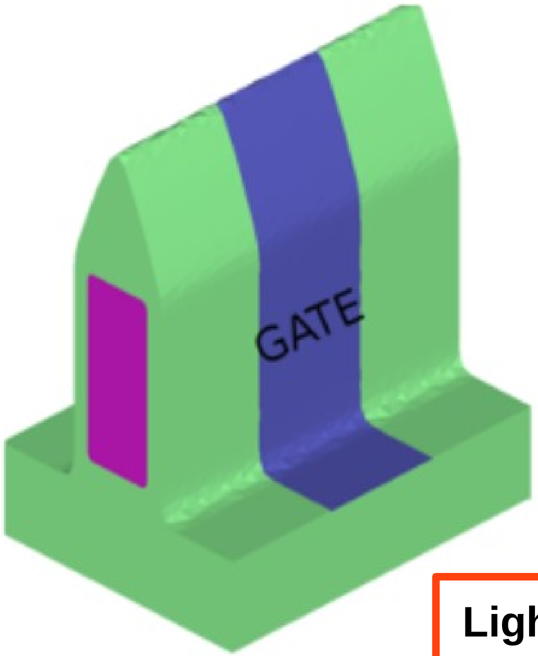
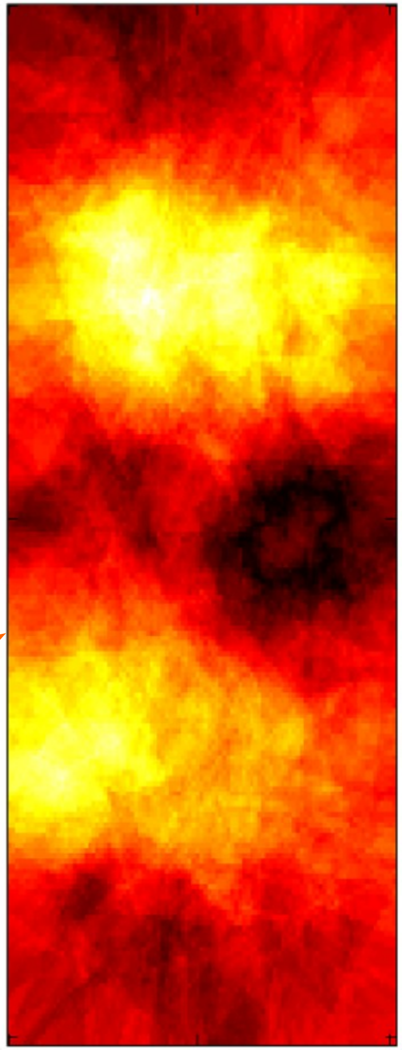
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



Light colour → **High** Sensitivity

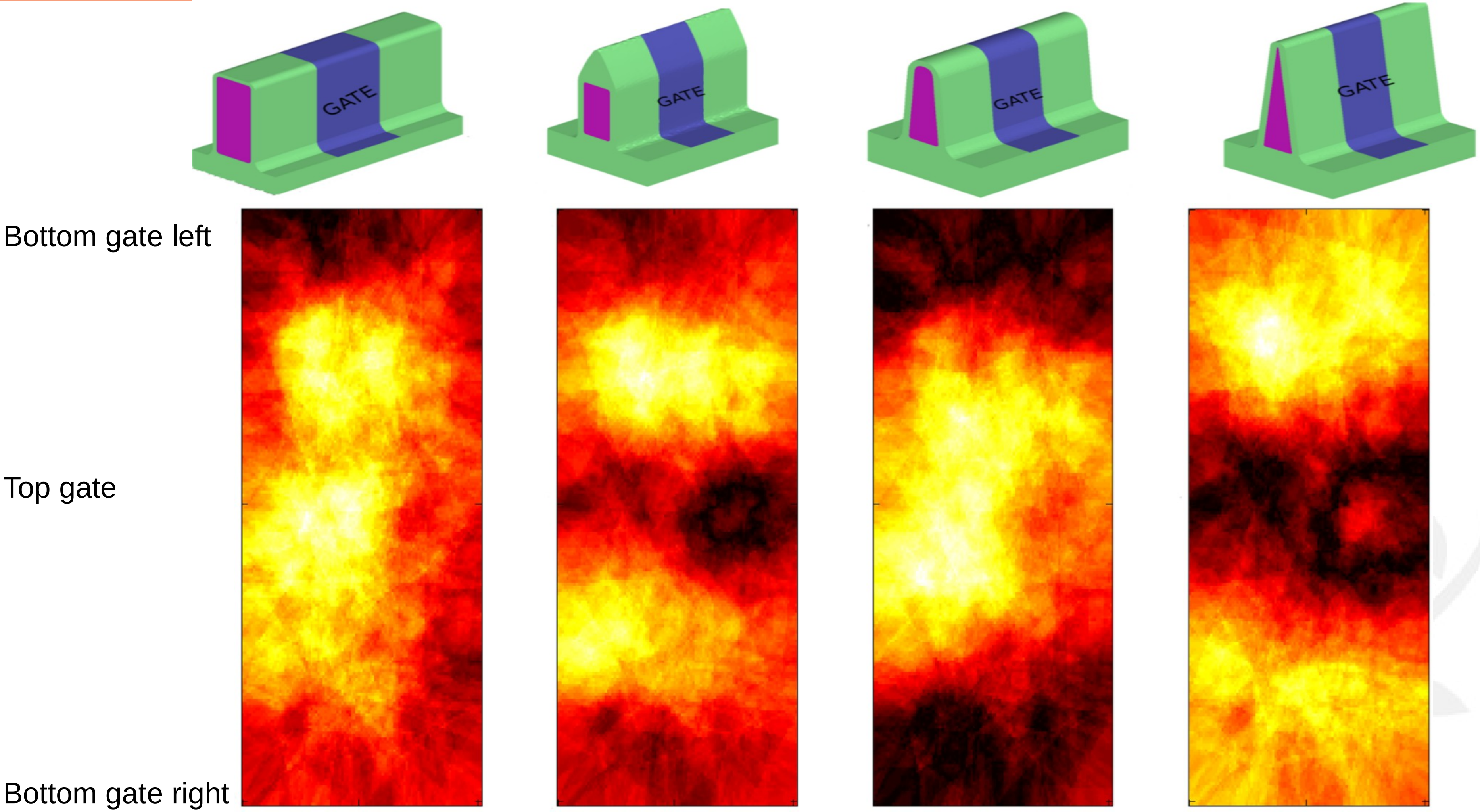
Dark colour → **Low** Sensitivity



Fluctuation Sensitivity Map

How can we know more?

Fluctuation Sensitivity Map (**FSM**)



Four FinFET devices with the **same dimensions** but **different shapes**

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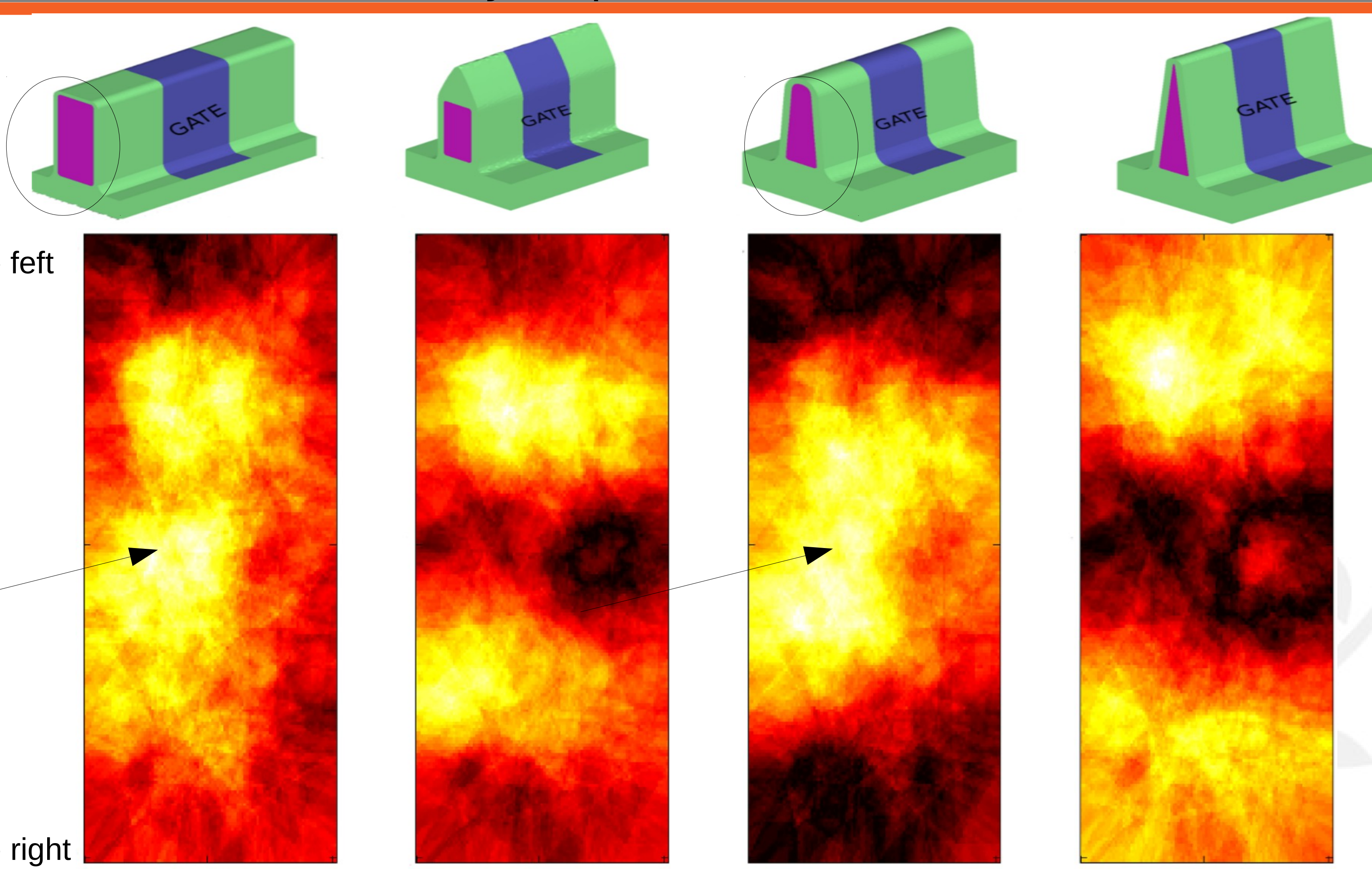
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



Bottom gate feft

Top gate

Bottom gate right

High Sensitivity → Top of the gate

Low Sensitivity → Bottom of the gate

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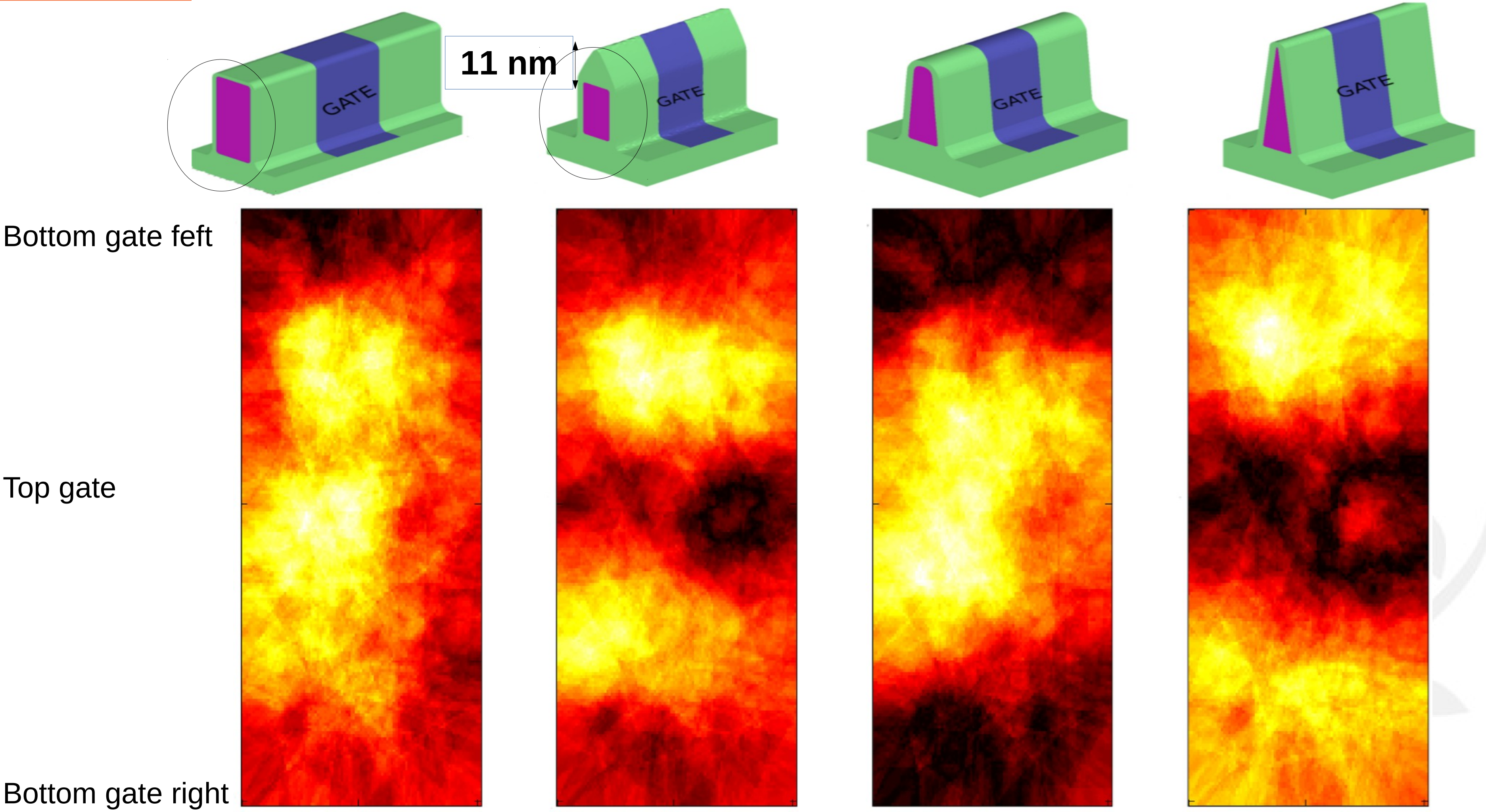
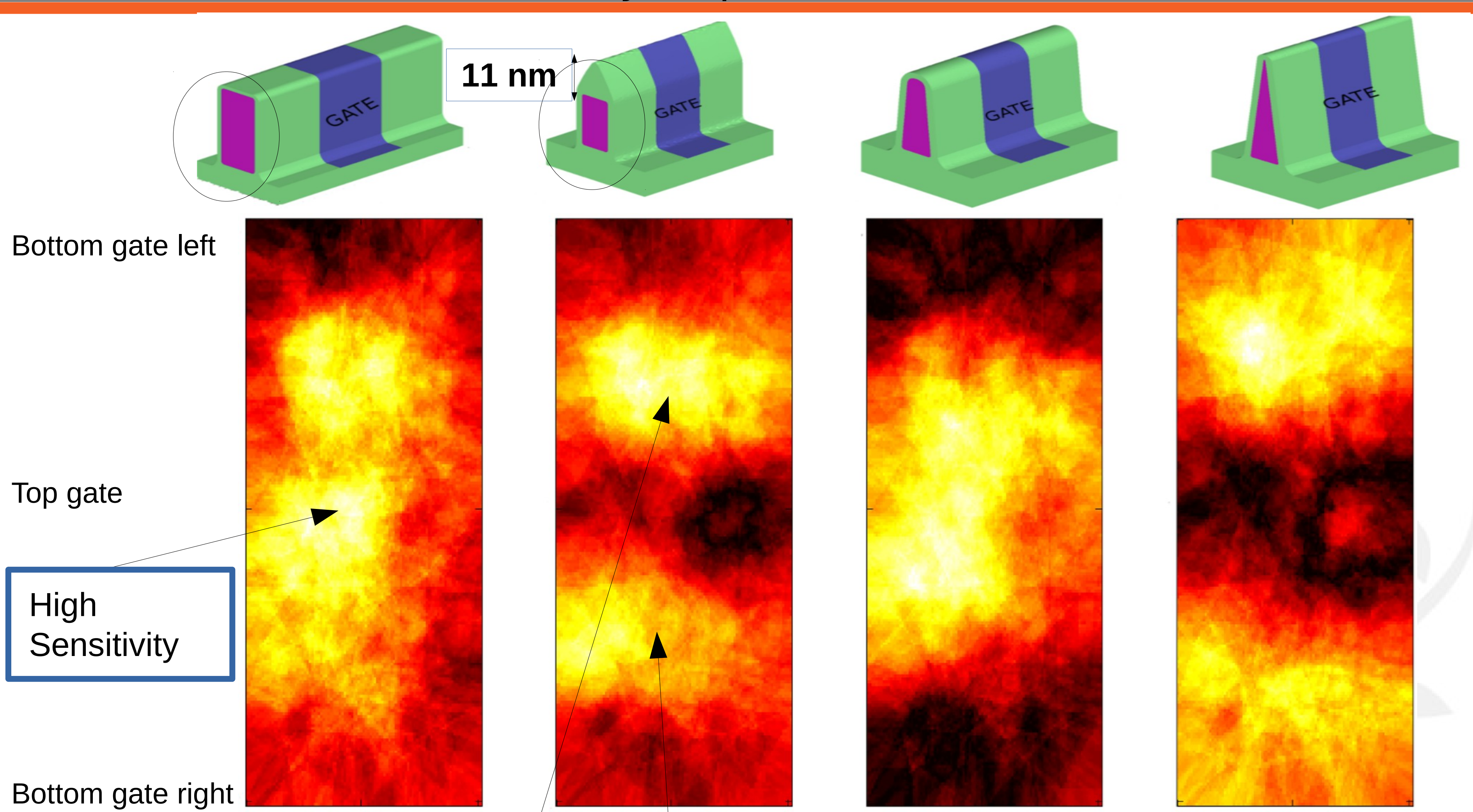
How can we know more?

Fluctuation Sensitivity Map (**FSM**)



How can we know more?

Fluctuation Sensitivity Map (**FSM**)



High Sensitivity → Sidewalls of the gate

Low Sensitivity → Top of the gate

Outline

- Motivation
- Simulation methodology
- Results
- **Conclusion**

Conclusion

- We have two **in-house built 3D finite-element simulation tools** based on the **drift-diffusion** and the **Monte Carlo** methods

- Using our simulation tools we can **introduce** new **materials**, device **structures**, **physical phenomena**...

- We have studied **promising candidates** for **future generation** transistor nodes, progressively scaling them in order to keep up with the **industry requirements**

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Conclusion

- We have **modelled** (with mathematical models), **implemented** (via simulations) and **analysed** (through statistical analysis) the **variability effects** that limit the **performance** and **reliability** of semiconductor devices

- We have **introduced** the variability sources as soon as they appear in the **new technological nodes**

- We have improved the previously existing method to model the **metal grain granularity** (Voronoi approach)

- We have tackled the **large computational cost** of variability studies (via the FSM and the GWM)

No lemons were harmed in the making of this work

Thank you for your attention