On-Chip Solar Cell and PMU on the Same Substrate with Cold Start-Up from nW and 80 dB of Input Power Range for Biomedical Applications

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***Abstract*—This paper presents a 1 mm^2 solar cell and a Power Management Unit (PMU) on the same substrate to rise up the harvested voltage above 1.1 V to power wearable or implantable devices. The on-chip solar cell and the PMU are fabricated in standard 0.18 μm CMOS technology achieving a form factor of 1.575 mm^2. Experimental results show that the PMU is able to start-up from a harvested power of 2.38 nW without any external kick off or control signal and can handle a harvested power up to μW with a continuous and two-dimensional Maximum Power Point Tracking (MPPT) that works in open-loop mode to set the frequency, the gain and the capacitor sizes of a charge pump.**

I. Introduction

Micro-energy harvesting with a solar cell and a Power Management Unit (PMU) on the same substrate results in a very small form factor and reduced costs [1], [2]. This approach leads to two main design challenges. First, the scavenged power can be as low as a few nW. This makes it difficult to work without external control signals or start-up mechanisms [2]. Second, it is hard to handle a wide input power range with a significant energy efficiency [3]. As an example, the input power for an on-chip solar cell of 1 mm^2 vary from a few nW to several μW for an illumination range from 100 lx to 100 klx [4]. This calls for an efficient PMU with Maximum Power Point Tracking (MPPT) consuming nW.

This paper presents a PMU powered by a 1 mm^2 on-chip solar cell to rise up the harvested voltage above 1.1 V while driving on- or off-chip capacitors which would act as energy reservoirs. The proposed micro-energy harvesting proof-of-concept chip is intended for biomedical implantable devices located in body areas exposed to light such as inside the eye or under the skin, as the form factor is a constraint, and the absence of an external control avoids off-chip companion conditioning circuits of the harvester. The main contributions of this paper are:

- An on-chip solar cell and a PMU on the same substrate in standard CMOS technology
- A self-powered PMU capable of starting up from 2.38 nW with an on-chip solar cell of 1 mm^2 in standard 0.18 μm CMOS technology and without any external kick-off or control signal

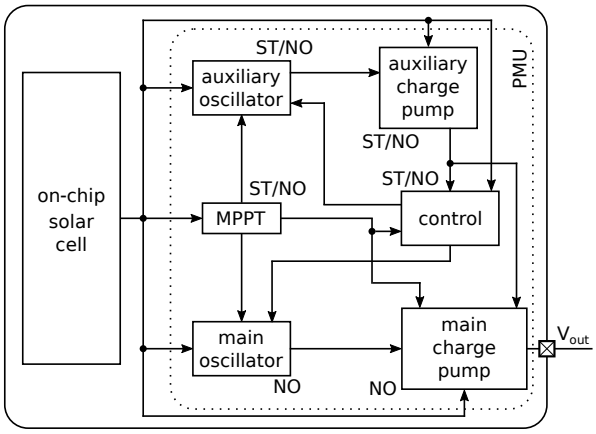

Fig. 1. Architecture of the proposed micro-energy harvesting chip with a PMU and an on-chip solar cell on the same substrate.

- A continuous, two-dimensional and open-loop MPPT which searchs for the maximum power across an input range of nW to μW through the change in the topology of a capacitive DC/DC converters and its switching frequency

II. Proposed Architecture

Fig. 1 shows the proposed architecture. The PMU features two operation modes, namely, start-up and normal operation. NO and ST/NO labels in Fig. 1 indicate the functional blocks active in normal mode and in both modes respectively. Our approach comprises an on-chip solar cell as a P^+ over P-well in N-well over P-substrate of 1 mm^2 photodiode that supplies the energy of the PMU, which, in turn, is made up of an auxiliary oscillator driving an auxiliary charge pump that provides the voltage levels of the control circuit and the main charge pump switches. The main oscillator and DC-DC converter are OFF during the start-up process by means of power gating to cut energy consumption. The auxiliary DC-DC converter starts working when the voltage generated by the photodiode, V_{PD}, is high enough to switch on the auxiliary oscillator and to trigger the start-up process (in our design this voltage was measured to be 0.17 V). The output voltage of the

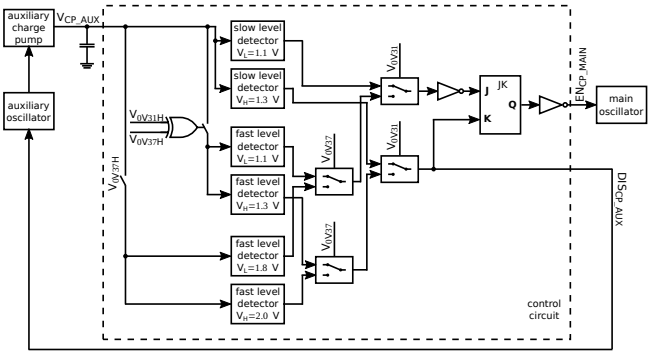

Fig. 2. Control circuit of our proof-of-concept harvester chip.

system, V_{out}, is provided by the main DC-DC converter, which yields a voltage level above 1.1 V during the normal operation phase of the PMU.

The MPPT block works in open-loop, continuous and two-dimensional mode, so it is always connected to the photodiode. Our MPPT approach is inspired by the Fractional Open Circuit Voltage (FOCV) method since the maximum power point is tracked through the photodiode voltage, V_{PD}. Nevertheless, in our case the PMU is not disconnected from the photodiode, i.e. we do not measure the photodiode open circuit voltage. The MPPT block is designed to meet the maximum PMU efficiency adjusting both the gain and the capacitance per stage of the main charge pump and the clock signals' frequency of both charge pumps. A joint analytical model of photodiode and charge pump [4], [5] has been used to predict the photodiode response, searching for the maximum load which yields 1.1 V at the PMU output during the design phase. So, our MPPT method can be regarded as a lookup table defined in the design phase. This MPPT strategy leads to ultra-low power consumption allowing the PMU to start-up from 2.38 nW. Four level detectors have been designed to distinguish among five different working regions (WR1-WR5) are defined in the design phase for the MPPT to cover the voltage range of the photodiode. Their nominal trigger voltages were finally set to V_{0V25} = 0.25 V, V_{0V31} = 0.31 V, V_{0V37} = 0.37 V and V_{0V42} = 0.42 V.

Fig. 2 shows the architecture of the control circuit. The control circuit limits the output voltage of the auxiliary charge pump, V_{CP_AUX}, to cut power consumption. It also determines when the auxiliary and main oscillators and charge pumps are ON through power gating. This is performed with two different threshold voltage levels in signals V_{CP_AUX}, V_L and V_H, that are set through voltage level detectors. The values of V_L and V_H depend on the illumination. Their nominal values have been designed to be 1.1 V and 1.3 V, respectively, for low and medium illuminations (working regions WR1-WR3), and 1.8 V and 2.0 V for high illumination (working regions WR4-WR5). The reason to work with higher voltage levels for high illumination is to decrease the conduction losses in the switches of the main charge pump. To further increase the efficiency we optimized the trade-off between consumption and detection speed, so that for low illumination

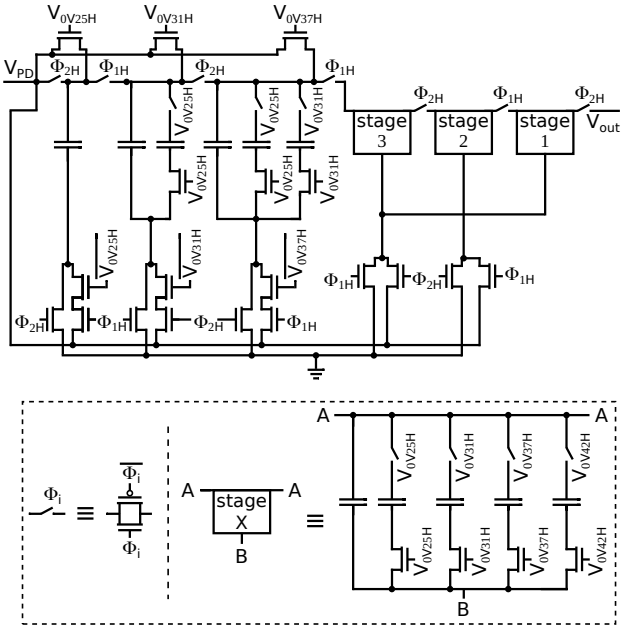

Fig. 3. Schematic of the main DC/DC converter of our proof-of-concept harvester chip.

we designed slow and very low-power level detectors (WR1-WR2), whereas the opposite for medium and high illumination (WR3-WR5). The control circuit also comprises a JK flip-flop to separate start-up from normal operation. In normal operation, the main oscillator is ON while $V_{CP\_AUX} > V_L$, and OFF during the start-up process until $V_{CP\_AUX} > V_H$.

III. Circuit Implementation

The main DC-DC converter, based on a Dickson charge pump with transmission gates as switches and with variable gain and capacitance per stage, is shown in Fig. 3. Its two non-overlapping clock signals are generated by the main oscillator. The control signals to modify the structure of the converter are provided by the level detectors of the MPPT block according to V_{PD}. Also, level shifters based on [6] are added between the level detectors within the MPPT block (see Fig. 1) and the main oscillator to provide higher voltages V_{0V25H}, V_{0V31H}, V_{0V37H}, V_{0V42H} and clock signals Φ_{1H}, Φ_{2H} from signals V_{0V25}, V_{0V31}, V_{0V37}, V_{0V42} and Φ_1, Φ_2, rising them up to the V_{CP_AUX} level, for the right operation of the main charge pump switches. The gain and the capacitance per stage were designed with the circuit models introduced in [4], [5]. The reconfigurable values of the gain of the main charge pump are 7× with 100 pF per stage for WR1, 6× with 200 pF for WR2, 5× with 400 pF for WR3, 4× with 600 pF for WR4 and 4× with 750 pF for WR5. The capacitors used for high illumination are made with PMOS transistors (PCAPs) to shrink area, while the stages that are active for low illumination are PCAPs and MIM devices connected in parallel to reduce leakage currents.

The auxiliary charge pump is a Pelliconi circuit [7] of 8 stages with NMOS transistors in P-well as diodes to avoid the substrate effect and increase the efficiency of the converter, and thus, that of the start-up phase. The capacitors are implemented

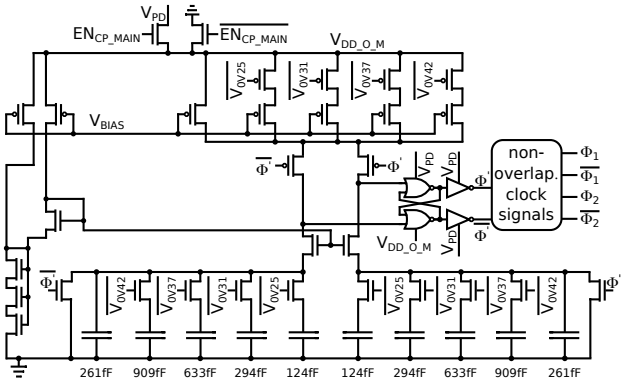

Fig. 4. Schematic of the main oscillator.

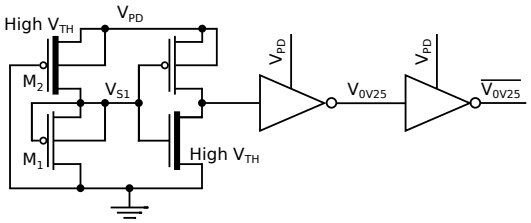

Fig. 5. Schematic of a level detector of the MPPT block.

with MIM structures to maintain low leakage currents. The converter has a fixed gain and capacitance per stage, so the frequency of the clock signal is the only way to adjust the output power of the converter according to the illumination.

The main and auxiliary oscillators are relaxation oscillators based on [8]. As Fig. 4 depicts, different branches with different capacitor sizes driven by the four level detectors of the MPPT block described in Section II adjust the frequency of the main oscillator. In addition, voltage V_{BIAS} which changes with voltage V_{PD}, i.e. with the illumination, further adjusts the frequency of the main oscillator. The current used for the generation of voltage V_{BIAS} varies from 50 pA for $V_{PD} = 0.2$ V up to 4 nA for $V_{PD} = 0.5$ V. The resultant frequency of the main oscillator by combining the two methods varies continuously from 100 Hz to 150 kHz. The frequency of the auxiliary oscillator changes in the range 1.5 kHz to 500 kHz through V_{BIAS}.

The trigger voltage of every level detector of the MPPT block is set by a PMOS cascode structure [9] through the currents drawn by transistors M_1 and M_2 in Fig. 5. These voltages (V_{0V25}, V_{0V31}, V_{0V37}, or V_{0V42}) are defined by adjusting the dimensions of transistors with different threshold voltages. A cascade of three inverters sharpen the transition between MPPT working regions.

IV. Experimental Results

A proof-of-concept chip was fabricated in standard 0.18 µm CMOS technology, with an on-chip solar cell of 1 mm^2 powering a PMU on the same silicon substrate. The result features a form factor of 1.575 mm^2. Fig. 6 shows a photograph of the 5×5 mm^2 micro-energy harvesting chip with several test structures to study effects like the impact of fingers on the photodiode which acts as solar cell. It was seen

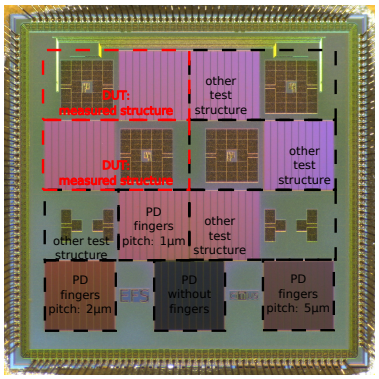

Fig. 6. Die micrograph of the 5×5 mm^2 micro-energy harvesting chip with different structures for testing.

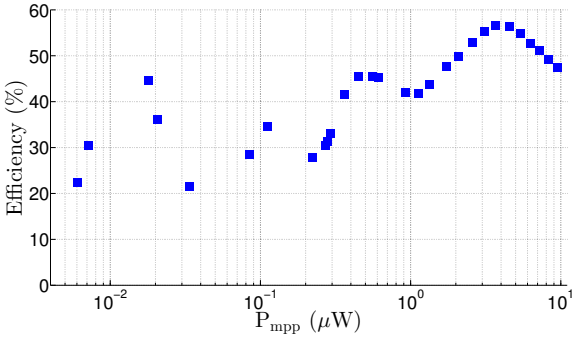

Fig. 7. Measured end-to-end efficiency for different input powers.

that photodiodes with fingers of 1 µm pitch provide higher power than other photodiodes without fingers or with different pitches. The generated voltage of such on-chip photodiodes is in the range [0.27, 0.46] V for an illumination span of 100 lx to 100 klx, and a harvested power between 3.7 nW and 8.3 µW for the same illumination range.

The end-to-end measured efficiency defined by $\frac{P_{out}}{P_{mpp}}$ is shown in Fig. 7, where P_{mpp} is the maximum power generated by the photodiode and P_{out} is the PMU output power. To obtain P_{mpp}, the PV curve of an isolated on-chip solar cell is measured with an SMU. Simultaneously, another SMU measures P_{out}. The efficiency is above 20% and 40% for low and high input powers, respectively, reaching a peak of 57% in between. Several factors contribute to the ripple in the efficiency. First, a discrete number of working regions causes ripple by itself. Second, the mismatch between the doping profiles of the photodiode provided by the manufacturer and the actual ones contributes to the ripple too. Also, possible oscillations caused by the lack of hysteresis in the MPPT level detectors add to the ripple. The lower efficiency for very low illumination is natural and it comes from the fact that the transistors are slower and more power hungry in this regime.

Table I shows that there is no prior work reported in the literature with the energy harvester transducer and the PMU with MPPT on the same substrate capable of handling around 80 dB of input power range while starting-up from 2.38 nW without external kick-off. The key to achieving such a performance is the open-loop MPPT due to its low

TABLE I
EXPERIMENTAL DATA SUMMARY OF OUR PROOF-OF-CONCEPT CHIP AND STATE-OF-THE-ART

	[2]	[10]	[11]	[12]	[3]	This Work
Technology	standard 0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	standard 0.18 μm CMOS
Voltage boosting	charge pump	boost with voltage doubler	self-oscillating voltage doubler	charge pump	discontinuous charge pump	charge pump
Transducer + PMU on-chip	yes	no	no	no	no	yes
Transducer + PMU area (mm^2)	1.3 + 0.24	? + 1.53	? + 0.86	? + 0.552	? + 2.72 + off-chip cap.	1 + 0.575
Input power range (nW)	-	1.1 - 6.25	1.7 - 12500	5900 - 47000	0.02 - 1500	2.38 - >10000
Output power range (nW)	-	0.544 - 4	0.5 - 5000	3840 - 30550	0.005 - 600	0 - 4500
Cold start-up	yes	no	yes	yes	no	yes
Minimum input power to start-up (nW)	-	-	6	-	-	2.38
MPPT	no	no	user-operated	yes	yes	yes
Output regulation	no	no	no	yes	no	no
End-to-end peak efficiency (%) @ P_{out} (μW)	67@1.27	53@0.0012	50@0.12	72@-	50@0.008	57@2.07

power consumption. Further improvements could be met by refining the joint model of the photodiode and the capacitive charge pump used for defining the different working regions using experimental results. The reduced form factor from the energy transducer and the PMU on the same substrate is of interest for biomedical applications like implantable devices [1]. Table I also shows that the solution in [2] comprises a transducer and a PMU on the same substrate without MPPT. The work in [10] includes an external inductor and it does not incorporate MPPT. In [11] a self-oscillating voltage doubler reaches high peak efficiency without MPPT as the authors manually change the gain by adjusting the number of cascaded stages of voltage doublers. The charge pump in [12] yields high efficiency with MPPT and cold start-up, however it is not intended for micro-energy harvesting since the minimum input power needed is about μW with an input voltage around 1 V. Finally, [3] introduces the discontinuous charge pump concept achieving good efficiency, nevertheless the chip needs an external capacitor and it does not have cold start-up.

V. CONCLUSION

A new micro-energy harvesting system for biomedical applications with a 1 mm^2 solar cell and a PMU on the same substrate has been designed and fabricated in standard 0.18 μm CMOS technology. The PMU includes a continuous and open-loop MPPT which defines five different working regions depending on the illumination. Experimental results demonstrate a good efficiency for a high input power range of 80 dB. The system is able to start-up from 2.38 nW of harvested power without any external kick-off or control signal.

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