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Ultra-low power voltage reference circuit for implantable devices in standard CMOS technology

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Summary

An ultra-low power CMOS voltage reference for body implantable devices is presented in this paper. The circuit core consists of only regular threshold voltage PMOS transistors, thus leading to a very reduced output voltage dispersion, defined as σ/μ, and extremely low power consumption. A mathematical model of the generated reference voltage was obtained by solving circuit equations and its numerical solution has been validated by extensive electrical simulations using a commercial circuit simulator. The proposed solution incorporates a passive RC low-pass filter, to enhance power supply rejection (PSR) over a wide frequency range, and a speed-up section, to accelerate the switching-on of the circuit. The prototype was implemented in 0.18 μm standard CMOS technology and is able to operate with supply voltages ranging from 0.7 V to 1.8 V providing a measured output voltage value of 584.2 mV at the target temperature of 36 °C. The measured σ/μ dispersion of the reference voltage generated is 0.65% without the need of trimming. At the minimum supply of 0.7 V the experimental power consumption is 64.5 pW, while the measured PSR is kept below -60 dB from DC up to the MHz frequency range.

KEYWORDS:
voltage reference, ultra-low power, picowatt, subthreshold, trim-free, design methodology

1 | INTRODUCTION

Voltage reference circuits are basic building blocks in many analog and mixed-signal circuits such as, for example, voltage regulators, analog to digital converters (ADCs) or biasing circuits of analog amplifiers. Typically, they belong to the always-on part of the system and hence, limiting their power consumption is of great importance to improve the overall power budget. This is particularly critical in applications where the use of rechargeable batteries is not possible, such as for example in certain types of biomedical implantable devices, or in applications where the available power supply is severely limited, as it is the case of wearable devices or remotely deployed nodes in the context of Internet of Things (IoT). In these cases, it is of utmost importance to reach ultra-low power consumption to have autonomous systems or to extend battery life.

Conventional solutions make use of the bandgap voltage reference (BGR) exploiting the existence of parasitic bipolar junction transistors (BJTs) in standard CMOS technologies[1,2,3,4]. The rationale behind BGR is based on the combination of two different voltages, one with proportional-to-absolute temperature (PTAT) characteristics and one with complementary-to-absolute-temperature (CTAT) in order to compensate drain current variations and generate a voltage reference which is independent of temperature. The main drawback of these approaches is that solutions with reduced power consumption typically require a substantial area overhead or present poor temperature stability[4].

To achieve ultra-low power consumption in CMOS technology, subthreshold operation transistors are used to implement voltage reference circuits. Two main approaches exist based on either the difference between transistors threshold voltages [5,6,7,8,9] or on different current densities [10,11,12]. The implementations based on threshold voltages difference have, in general, very low power consumption with good power supply rejection (PSR) and line sensitivity (LS) performance, but suffer from process variations due to the explicit dependency of the generated reference voltage with the transistors threshold voltage. For this reason, they normally need a post-fabrication trimming of each chip to reduce the effect of process spreads. In addition, some of these approaches [5,7] use different types of transistors to generate the different threshold voltages, which requires more fabrication steps increasing overall process variations. In reference [13] a trim-free implementation using only PMOS transistors is proposed which modulates the transistor threshold voltage by body effect through modifications of the source-bulk voltage. In so doing, the reference voltage obtained with this structure is threshold voltage independent under certain assumptions, and by properly sizing the circuit transistors it is possible to obtain good process variations, robustness and achieve temperature compensation. Alternatively, it is possible to tune the threshold voltage by means of modifications at device-level such as gate doping [14] or channel implants [15], but these approaches are not compatible with standard CMOS fabrication processes. On the other hand, in the subthreshold voltage reference circuits based on different current densities [10,11,12], the reference voltage is generated by the difference in gate-source voltages produced by a current flowing across two transistors with different W/L ratio [1], resulting in a PTAT voltage. These references are not threshold voltage dependent on first approximation but suffer from strong temperature-dependency. If a wide temperature working range is needed, a compensation circuit has to be incorporated, resulting in high area and power consumption.

In this paper an ultra-low power reference voltage using only regular transistors in 0.18μm standard CMOS technology based on contribution [13] is proposed, with a total silicon area of 1830 μm^2 and an experimental power consumption of 64.5 pW at 0.7 V of supply voltage and 36 °C of temperature. The proposed solution achieves a measured average PSR of at least -60 dB up to frequencies of MHz and an output voltage dispersion, defined as the ratio σ/μ, of only 0.65 % without trimming. The circuit is intended to be used in implantable devices and therefore the design constraints are a small form factor and ultra-low power consumption while other considerations such as the temperature coefficient are less critical. In order to ease the design process, a mathematical circuit model is proposed based on the circuit equations. The model has been validated through electrical level simulations using a commercial design environment with a 0.18μm CMOS fabrication process. The obtained results are in agreement with experimental data from fabricated devices.

In Section 2, the core of the proposed voltage reference circuit is presented and the mathematical model of the circuit is developed and validated. Based on this analysis we present, in Section 3, an ultra-low power voltage reference circuit consisting of the reference voltage generator core, a passive low-pass filter for high-frequency PSR improvement and a speed-up mechanism. In addition, the design methodology followed for the exploration of the design space is also presented. In Section 4, measurement results of 40 samples of the proposed circuit contained in 20 chips are shown, together with a comparison of the main figures of merit of the proposed approach with state-of-the-art solutions. Finally, the conclusions drawn can be found in Section 5.

2 | PMOS-ONLY V_{REF} CORE

We take as reference the circuit shown in Figure 1 , which was first introduced in [13]. The circuit operating principle is based on the threshold voltage modulation due to body biasing of transistor M_1. Across transistor M_4 a subthreshold current flows which depends on the W/L ratio of the device. Diode connected transistor M_3 acts as a current-to-voltage converter to generate the voltage V_{body}. The voltage V_{body} determines the drain current of M_1, by threshold voltage modulation, which passes through diode connected transistor M_2 generating the reference voltage of the circuit, V_{ref}.

The analysis carried out in [13] neglects the current flowing through the parasitic diode formed by the source-bulk PN junction of transistor M_1, as it is said to be three orders of magnitude smaller than the drain current of transistor M3. In our case, considering four regular transistors of the same type in the selected technology, this assumption is not feasible because the current of the parasitic diode, I_{SBM1} in Figure 1 , has a value of the same order of magnitude as the drain current of transistor M_3, according to electrical simulations. The rationale of using four regular threshold voltage PMOS transistors as opposed to other possible combinations such as regular and low-V_t transistors is twofold. On the one hand, being of the same type a reduced output voltage dispersion, defined as σ/μ, can be obtained while, on the other hand, ultra-low power consumption is ensured by minimizing the transistor's drain current with respect to low-V_{th} alternatives. For this reason, in our proposal an analysis of the circuit considering the current I_{SBM1} will be performed and validated by means of extensive simulations.

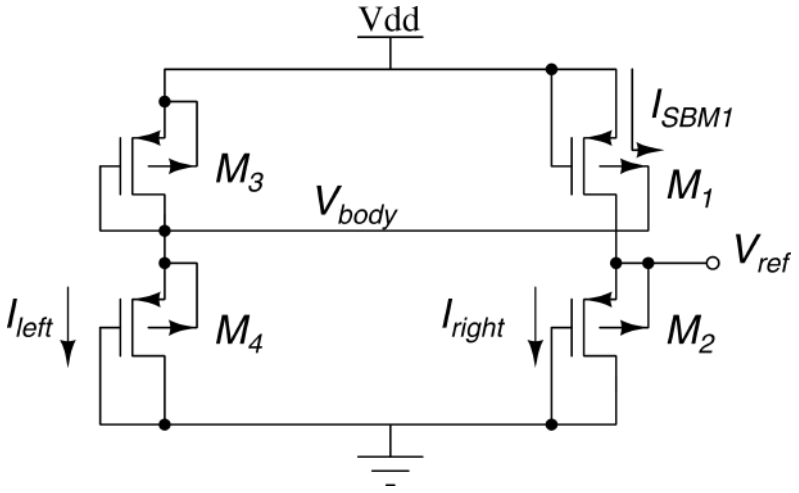


FIGURE 1 Core of the reference voltage generator.

2.1 | Fundamental equations

Next and for the sake of completeness, we will summarize the main transistor equations that will be used in our analysis of the V_{ref} core in order to derive a mathematical expression for the calculation of the generated reference voltage.

The drain current of a PMOS transistor operating in weak inversion can be expressed as (1),

$$I_D = I_s \frac{W}{L} e^{\frac{V_{sg}+V_{th}}{nV_T}} (1 - e^{\frac{-V_{sd}}{V_T}}) \simeq I_s \frac{W}{L} e^{\frac{V_{sg}+V_{th}}{nV_T}} \tag{1}$$

where $I_s = 2n\mu_p C_{ox} V_T^2$ is the characteristic current, $n = 1 + \frac{\gamma}{2\sqrt{V_{BS}+2|\Phi_F|}}$ is the subthreshold slope factor, μ_p is the hole mobility, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ the gate capacitance per unit area with ϵ_{ox} the gate oxide permittivity and t_{ox} the gate oxide thickness, $\gamma = \frac{\sqrt{2q_e\epsilon_{Si}N_{ch}}}{C_{ox}}$ is the body effect parameter with N_{ch} the channel bulk doping concentration and $|\Phi_F| = V_T ln(\frac{N_{ch}}{n_i})$ is the bulk Fermi potential being n_i the intrinsic carrier concentration, and $V_T = \frac{kT}{q}$ the thermal potential where k is the Boltzman constant, T the absolute temperature and q the electron charge [16,17]. If the source-drain voltage is equal to or greater than $4V_T$ (around 100 mV at room temperature), the transistor operates in saturation and the term $e^{\frac{-V_{sd}}{V_T}}$ in (1) can be neglected.

The source-bulk current of a PMOS transistor can be expressed by the regular PN junction current equation as (2),

$$I_{SB} = I_{D0} \cdot (e^{\frac{V_{sb}}{n_j V_T}} - 1) \tag{2}$$

where I_{D0} is the reverse saturation current of the junction and n_j is a parameter known as the junction emission coefficient, typically close to 1. The term I_{D0} can be calculated as $I_{D0} = J_s \cdot A_s + J_{ssw} \cdot P_s$, where J_s is the junction saturation current density, J_{ssw} is the sidewall junction saturation current density, A_s is the source junction area and P_s is the perimeter of the source junction. J_s and J_{ssw} are technology dependent parameters, while A_s and P_s depend on the transistor channel width, W, and on the length of the source diffusion, E. The area and perimeter of the source-bulk PN junction can be calculated as $A_s = W \cdot E$ and $P_s = 2 \cdot (W + E)$, respectively.

On the other hand, the dependency of the threshold voltage for PMOS transistors with the source-bulk voltage takes the general form of (3) [17], where V_{th0} is the threshold voltage of the transistor when its source and bulk terminals are shorted, that is, for V_{SB} equal to zero.

$$V_{th} = V_{th0} - \gamma \left(\sqrt{2|\Phi_F| - V_{SB}} - \sqrt{2|\Phi_F|} \right) \tag{3}$$

The dependency of the threshold voltage V_{th0} with channel dimensions can be expressed as (4) [18],

$$V_{th0}(W, L) = V_{th0GR} + D_{l1} \left(\frac{1}{L_{GR}} - \frac{1}{L} \right) + D_{l2} \left(\frac{1}{L_{GR}^2} - \frac{1}{L^2} \right) + D_w \left(\frac{1}{W_{GR}} - \frac{1}{W} \right) \tag{4}$$

where D_{l1},D_{l2} and D_w are technology parameters and V_{th0GR} is the threshold voltage of a geometry reference (GR) transistor M_{GR} with channel width W_{GR} and channel length L_{GR}.

2.2 | Numerical model

In [13] the analytical expression in equation (5) for the reference voltage, V_{ref}, generated by the circuit in Figure 1 was derived. This analysis, however, neglects the bulk current of transistor M_1 as well as other second-order effects, such as transistor sizing impact on the threshold voltage or subthreshold slope factor modulation by bulk voltage.

$$V_{ref} = \gamma \left(\sqrt{2|\Phi_F| - nV_T ln\frac{W_4 L_3}{W_3 L_4}} - \sqrt{2|\Phi_F|} \right) + nV_T ln\frac{W_1 L_2}{W_2 L_1} \tag{5}$$

Taking as reference this circuit architecture and with the aim of reducing the overall power consumption, the current through M_4 transistor has to be decreased, thus reducing the current through M_3 as well. In so doing, the source-bulk current of M_1, I_{SBM1}, can not longer be neglected, as this diode current can reach the amount of several picoamperes with sufficient $V_{dd} - V_{body}$ voltage or enough temperature. As an example, in a particular implementation at 36 °C, the simulated source-bulk PN junction current of M_1 and the drain current of M_3 are both equal to 12 pA. Under this condition equation (5) is no longer valid. For this reason, a mathematical expression for V_{ref} taking I_{SBM1}, as well as second-order effects related to transistors sizing, into account will be derived in this section applying equations (1),(2),(3) and (4) to the circuit under study.

Applying (1) and (2) to the four transistors of the circuit in Figure 1 , assuming that M_1, M_2 and M_4 are in saturation, we have:

$$I_{DM1} = 2n_1 \mu_p C_{ox} V_T^2 \frac{W_1}{L_1} e^{\frac{V_{th1}}{n_1 V_T}} \tag{6a}$$

$$I_{DM2} = 2n_2 \mu_p C_{ox} V_T^2 \frac{W_2}{L_2} e^{\frac{V_{ref} + V_{th2}}{n_2 V_T}} \tag{6b}$$

$$I_{DM3} = 2n_3 \mu_p C_{ox} V_T^2 \frac{W_3}{L_3} e^{\frac{V_{dd} - V_{body} + V_{th3}}{n_3 V_T}} (1 - e^{\frac{V_{body} - V_{dd}}{V_T}}) \tag{6c}$$

$$I_{DM4} = 2n_4 \mu_p C_{ox} V_T^2 \frac{W_4}{L_4} e^{\frac{V_{th4}}{n_4 V_T}} \tag{6d}$$

$$I_{SBM1} = I_{D0}(e^{\frac{V_{dd} - V_{body}}{n_j V_T}} - 1) \tag{6e}$$

As it may be observed in (6e), only the source-bulk current of M_1 is taken into account in the analysis as this is the only forward-biased PN junction. Reverse biased PN junctions in the circuit have values in the order of femtoamperes, three orders of magnitude below the drain currents and the forward biased PN junction between source and bulk in transistor M_1, so they are all neglected. On the other hand, the drain current of M_4 is the sum of the drain current of M_3 and the source-bulk diode current of M_1, hence

$$I_{DM4} = I_{DM3} + I_{SBM1} \tag{7}$$

Therefore, for the left branch of the circuit in Figure 1 we can write equation (8).

$$2n_3 \mu_p C_{ox} V_T^2 \frac{W_3}{L_3} e^{\frac{V_{dd} - V_{body} + V_{th3}}{n_3 V_T}} (1 - e^{\frac{V_{body} - V_{dd}}{V_T}}) + I_{D0}(e^{\frac{V_{dd} - V_{body}}{V_T}} - 1) - 2n_4 \mu_p C_{ox} V_T^2 \frac{W_4}{L_4} e^{\frac{V_{th4}}{n_4 V_T}} = 0 \tag{8}$$

For the right branch, the drain currents of M_1 and M_2 are equal, resulting in (9).

$$2n_1 \mu_p C_{ox} V_T^2 \frac{W_1}{L_1} e^{\frac{V_{th1}}{n_1 V_T}} = 2n_2 \mu_p C_{ox} V_T^2 \frac{W_2}{L_2} e^{\frac{V_{ref} + V_{th2}}{n_2 V_T}} \tag{9}$$

From (9) it is possible to derive an explicit expression for V_{ref} using equations (3) and (4) for the calculation of the threshold voltage of each transistor. We considered a reference transistor with $W_{GR}/L_{GR} = 50/50$ μm/μm while the value of V_{th0GR} is a technological parameter provided by the foundry. For M_2, the source-bulk voltage is zero and the second term in (3) vanishes, whereas for M_1 the threshold voltage is given by (10), where its dependence with $V_{dd} - V_{body}$ is made explicit. The term $V_{th01}(W_1, L_1)$ is the threshold voltage value of M_1 without body biasing including geometry effects given by equation (4).

$$V_{th1} = V_{th01}(W_1, L_1) - \gamma \left(\sqrt{2|\Phi_F| - (V_{dd} - V_{body})} - \sqrt{2|\Phi_F|} \right) \tag{10}$$

Using (9) and (10) an expression for V_{ref} in the presence of a non-negligible bulk current can be obtained,

$$V_{ref} = n_2 V_T \left[ln\left(\frac{n_1}{n_2}\right) + ln\left(\frac{W_1 L_2}{W_2 L_1}\right) \right] + \frac{n_2}{n_1} V_{th01}(W_1, L_1) - V_{th2} + \frac{n_2}{n_1} \gamma \left(\sqrt{2|\Phi_F| - (V_{dd} - V_{body})} - \sqrt{2|\Phi_F|} \right) \tag{11}$$

Since the subthreshold slope factor depends on the source-bulk voltage, we can assume that $n_2 = n_3 = n_4 = 1 + \frac{\gamma}{2\sqrt{2|\Phi_F|}}$, while $n_1 = 1 + \frac{\gamma}{2\sqrt{2|\Phi_F|-(V_{dd}-V_{body})}}$ will be, in general, different for each operating condition. However, if a high precision is not required, expression (11) can be simplified as (12) ignoring the dependency of n_1 with the source-bulk voltage and neglecting geometry influence in the threshold voltage.

$$V_{ref} \approx n_2 V_T ln\left(\frac{W_1 L_2}{W_2 L_1}\right) + \gamma\left(\sqrt{2|\Phi_F| - (V_{dd} - V_{body})} - \sqrt{2|\Phi_F|}\right) \tag{12}$$

Equations (11) and (12) provide an expression for the generated reference voltage. However, as equation (8) does not have an explicit solution for $V_{dd} - V_{body}$, it is necessary to use a numeric approach. For this reason, a C++ program has been implemented to calculate the reference voltage of the circuit. The calculus procedure is shown in **Algorithm** 1 and relies on the previous equations. The execution of **Algorithm** 1 involves user-defined parameters such as the sizes of the four transistors, M_1 to M_4, and the temperature of operation, T, as well as other technological and physical parameters. Based on them, other related parameters (C_{ox}, γ, ...) are calculated. Then, equation (8) is numerically solved using the Newton-Raphson method, thus providing the value of the voltage difference $V_{dd} - V_{body}$. Afterwards, the values of certain parameters of transistor M_1, which depend on this voltage drop, are calculated. Finally, equation (11) is solved and the value of V_{ref} is obtained.

Algorithm 1 C++ program structure for $V_{dd} - V_{body}$ and V_{ref} calculation

Program inputs:

- User-defined parameters: T, $\frac{W_1}{L_1}$, $\frac{W_2}{L_2}$, $\frac{W_3}{L_3}$, $\frac{W_4}{L_4}$
- Physical parameters: ϵ_{ox}, ϵ_{Si}, n_i
- Technology parameters: V_{th0}, J_s, J_{ssw}, n_j, E, t_{ox}, μ_p, N_{ch}, D_{l1},D_{l2}, D_w

Calculate:

- $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$
- $\gamma = \frac{\sqrt{2q_e\epsilon_{Si}N_{ch}}}{C_{ox}}$
- $\Phi_F = V_T ln(\frac{N_{ch}}{n_i})$
- $n_{2,3,4} = 1 + \frac{\gamma}{2\sqrt{|\Phi_F|}}$
- $V_{th2,3,4}$ applying equation (4)

Solve equation (8) by using Newton-Raphson method → $V_{dd} - V_{body}$

Calculate:

- $n_1 = 1 + \frac{\gamma}{2\sqrt{|\Phi_F|-(V_{dd}-V_{body})}}$
- $V_{th01}(W_1, L_1)$ applying (4)

Solve equation (11) and obtain V_{ref}

2.3 | Model validation

In order to validate the V_{ref} model proposed in Subsection 2.2, circuit-level simulations in a 0.18 μm CMOS technology using a commercial circuit simulator were compared with the V_{ref} models with and without considering the effect of I_{SBM1}, provided by equations (11) and (5), respectively. The values for γ and Φ_F were calculated using the technology parameters N_{ch} and t_{ox}, while the subthreshold slope factor used in equation (5) was calculated as $n = 1 + \frac{\gamma}{2\sqrt{2|\Phi_F|}}$. In equation (5), the term $nV_T ln(W_4 L_3 / W_3 L_4)$ is equivalent to $V_{dd} - V_{body}$ [13].

To assess the accuracy of the model predictions, different scenarios identified as case studies 1 to 6 in Table 1 have been analyzed. The corresponding results are shown in Table 2 . In each case, the dimensions of the transistors have been set so as to correspond to different ratios of currents I_{DM3} and I_{SBM1}. To validate the model we consider the situations when I_{SBM1} is either equal or smaller/larger than I_{DM3}. As it can be seen in Table 2 the results provided by our model outperform the model

TABLE 1 Case studies considered for the model validation.

Case study	W_1/L_1 (μm/μm)	W_2/L_2 (μm/μm)	W_3/L_3 (μm/μm)	W_4/L_4 (μm/μm)	Case description
1	15/15	2/10	2/15	150/3	$I_{DM3} > I_{SBM1}$ with low I_{SBM1}
2	22/5	2/10	2/15	300/1.5	$I_{DM3} > I_{SBM1}$ with high I_{SBM1}
3	15/15	2/10	2/50	150/3	$I_{DM3} \approx I_{SBM1}$
4	150/15	2/10	2/15	150/3	$I_{DM3} \approx I_{SBM1}$
5	150/15	2/10	2/50	50/3	$I_{DM3} < I_{SBM1}$ with low I_{SBM1}
6	150/15	2/10	2/50	150/3	$I_{DM3} < I_{SBM1}$ with high I_{SBM1}

in (5) in all cases. The mean percentage differences in the estimation of V_{ref} with respect to the results obtained with a circuit simulator are 6.74 % for equation (5) and 1.85 % for our model, equation (11). Using the simplified equation (12), the mean error obtained for the same case studies is 3.33%. On the other hand, the source-bulk voltage of transistor M_1, $V_{dd} - V_{body}$, calculated by means of the numeric solution presented in the previous section offers a mean error of 2.06 % with respect to simulation values, meanwhile equation (5) offers a 28.5 % deviation.

The mathematical model in (11) represents therefore a powerful tool for the *a priori* calculation of the output provided by the voltage reference circuit, V_{ref}, as a function of the dimensions of the transistors and process parameters from the target CMOS technological node.

TABLE 2 Comparison of the accuracy of the model in (5) and the model proposed in this work taking into account the body bias effect, equation (11), with respect to electrical simulations in 0.18 μm CMOS technology using a commercial circuit simulator.

Case study	Simulation				Model in [13], eq. (5)			Our model, eq. (11)		
	$V_{dd} - V_{body}$ (mV)	V_{ref} (mV)	I_{DM3} (pA)	I_{SBM1} (pA)	$V_{dd} - V_{body}$ (mV)	V_{ref} (mV)	V_{ref} error (%)	$V_{dd} - V_{body}$ (mV)	V_{ref} (mV)	V_{ref} error (%)
1	179.4	115.2	8.4	1.9	200.7	116.7	1.2	180	116.6	1.2
2	213	168.6	22.1	10.23	247.6	182.6	8.3	208.2	172.3	2.16
3	203.5	122.3	5.4	4.9	241.5	130.3	6.5	201.2	125	2.22
4	152.7	185.6	3.9	6.4	200.7	194.6	4.9	148.8	182.4	1.75
5	131.2	178.7	0.67	2.8	204.3	195.8	9.6	125.7	173.5	2.92
6	160.5	188	1.6	8.7	241.5	208.3	10.8	154.9	184.7	1.74

3 | PROPOSED VOLTAGE REFERENCE CIRCUIT

Based on the PMOS-only V_{ref} core circuit analyzed in the previous section, a voltage reference circuit using only regular transistors in standard 0.18 μm CMOS technology has been developed for its application in body implantable devices. The main objectives are to achieve a very low power consumption, low process sensitivity and good PSR, disregarding temperature dependency because in the context of implantable devices the temperature will remain approximately constant and equal to 36°C.

3.1 | Circuit description

Figure 2 shows the proposed circuit architecture. It is composed of a V_{ref} core, a passive RC low-pass filter and a speed-up circuit. The core of the reference voltage generator works as the circuit studied in Section 2, incorporating the stacked diode connected M_{21}, M_{22}, M_{23}, M_{24} transistors to obtain a higher reference voltage with the same current level through the right

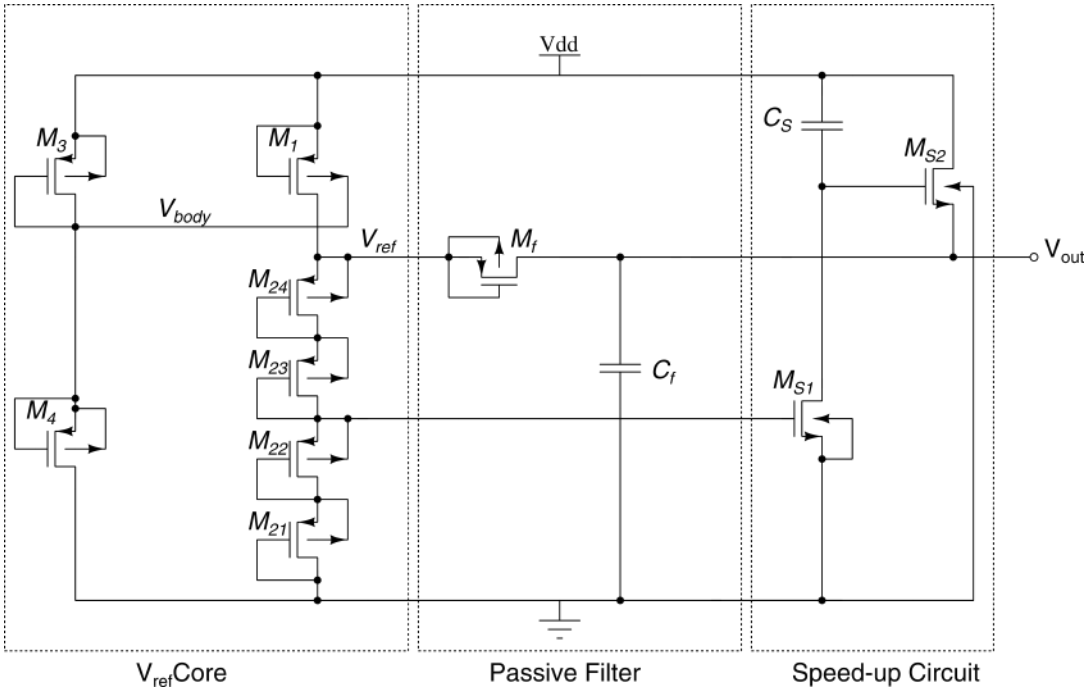


FIGURE 2 Proposed voltage reference circuit.

branch. As explained in Section 2.2, the impact of the reverse biased PN junctions of all transistors in the voltage reference core may be disregarded, as their current level is extremely low compared to the corresponding transistors drain currents. It is worth to point out that, even though the source-bulk PN junction of transistor M_1 is forward biased, there is no risk associated to this undesired parasitic device. Indeed, a forward biased source-bulk PN junction could lead to latch-up. Nevertheless, it may be observed in Table 2 that the value of the diode forward bias voltage, given by $V_{dd} - V_{body}$ and below 215 mV in any case, is not sufficient to activate the intrinsic diode in an effective way and, hence, to cause latch-up. Moreover, even if the value of $V_{dd} - V_{body}$ were larger in a particular design, there are technological strategies to reduce the latch-up risk at layout level[19].

The M_f transistor and C_f capacitor form an RC low-pass filter to improve high frequency PSR of the voltage reference as seen in[12]. In addition, a speed-up mechanism has been added given that due to the low current flowing through M_1 to maintain low power consumption and the high resistance of the filter transistor M_f, the time necessary to charge C_f capacitor can be excessively large, resulting in a high settling time. To minimize this effect, a simple speed-up circuit is proposed, which injects charge on the output node when the supply voltage is connected. The speed-up circuit consists of transistors M_{S1} and M_{S2} and capacitor C_S. When the supply voltage goes from 0 to V_{dd}, the gate voltage of M_{S2} reaches a value close to V_{dd} causing a voltage increase in V_{ref} due to the current through M_{S2}. Then, C_S capacitor is charged across M_{S1} decreasing M_{S2} gate voltage while M_{S1} gate voltage increases cutting off M_{S2} and isolating the output node from V_{dd}. As a consequence, a settling time improvement can be observed in Figure 3 , where simulation results are shown for the circuit transient response when a supply voltage of 1 V is applied at t=10 ms with and without the speed-up section and using a filter capacitor of $C_f = 1.54$ pF, value selected according the design procedure detailed later. As it can be seen, the 2% settling time for the reference voltage V_{ref} noticeably decreases from $t_{s,ns} = 1.04$ s to $t_{s,ws} = 40.3$ ms in this particular case, which represents a ×25 improvement. The aim of the speed-up circuit is simply to enhance the switching-on time of the output voltage and plays no role in setting the circuit operating point.

3.2 | High-frequency PSR improvement

As explained, the passive filter formed by M_f and C_f was designed to improve the high-frequency PSR response of the circuit. Next, we will derive an analytical expression for the PSR of the proposed solution based on the small signal model shown in Figure 4 by solving Kirchhoff current equations (13a), (13b) and (13c) for nodes Ⓐ, Ⓑ and Ⓒ respectively.

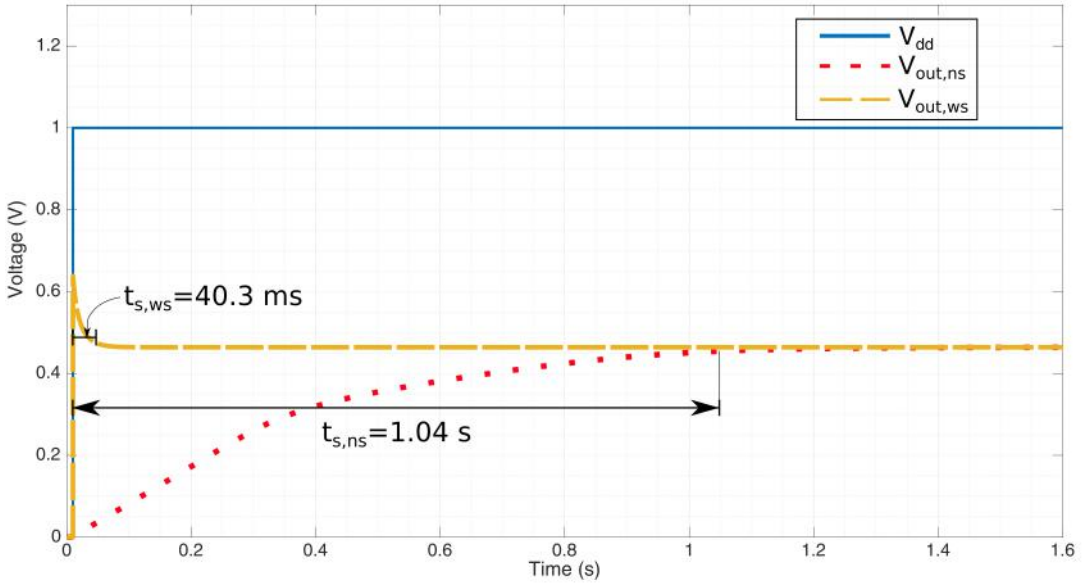


FIGURE 3 Transient simulation of the voltage reference in Figure 2 showing the effect of a sudden change of the supply voltage V_{dd} from 0 V to 1 V at $t = 10$ ms with no speed-up circuit ($V_{out,ns}$) and with speed-up circuit ($V_{out,ws}$) for a filter capacitor $C_f = 1.54$ pF.

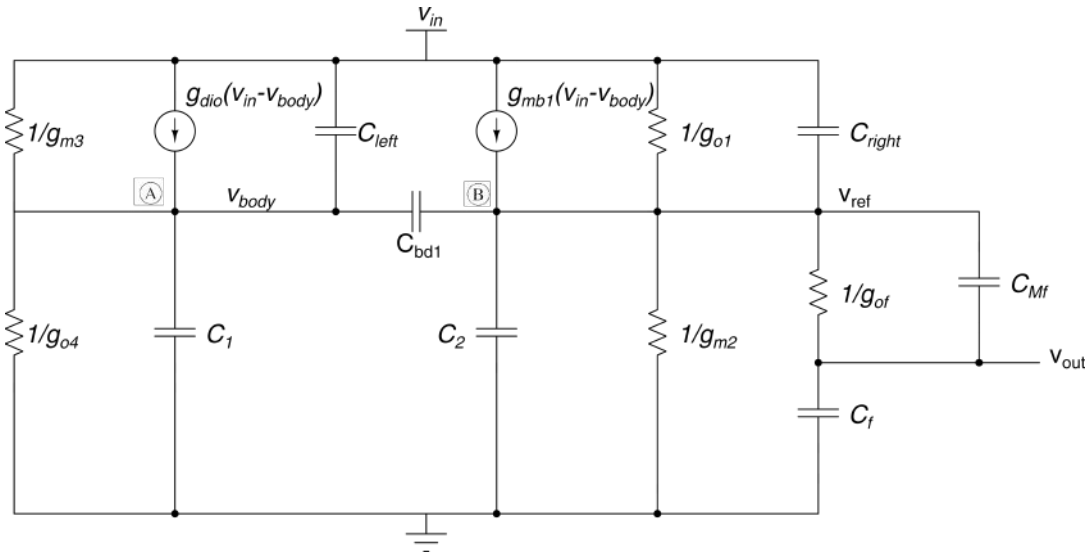


FIGURE 4 Equivalent small-signal model for the proposed circuit in Figure 2 .

$$g_{m3}\cdot(v_{in}-v_{body})-g_{o4}\cdot v_{body}+g_{dio}\cdot(v_{in}-v_{body})+s\cdot C_{left}\cdot(v_{in}-v_{body})+s\cdot C_{bd1}\cdot(v_{ref}-v_{body})\cdot-s\cdot C_1\cdot v_{body}=0 \quad (13a)$$

$$g_{mb1}\cdot(v_{in}-v_{body})+(g_{o1}+s\cdot C_{right})\cdot(v_{in}-v_{ref})-G_{m2}\cdot v_{ref}+(g_{of}+s\cdot C_{Mf})\cdot(v_{out}-v_{ref})+s\cdot C_{bd1}(v_{body}-v_{ref})-s\cdot C_2\cdot v_{ref}=0 \quad (13b)$$

$$g_{of}\cdot(v_{ref}-v_{out})+s\cdot C_{Mf}\cdot(v_{ref}-v_{out})-s\cdot C_f\cdot v_{out}=0 \quad (13c)$$

The C_{left} capacitor represents the capacitance between the input node and node (A) and can be approximated as the sum of the source-bulk capacitance of M_1 and the source-gate capacitance of M_3, $C_{left} \approx C_{sgM3} + C_{sbM1}$. C_{right} is the capacitance between the input and node (B), and can be approximated as the gate-drain capacitance of M_1, $C_{right} \approx C_{gdM1}$, while C_1 and C_2 are the capacitances seen from nodes (A) and (B) to ground, respectively, thus $C_1 \approx C_{gdM4} + C_{dbM4}$ and $C_2 \approx \frac{C_{gsM2x}+C_{bdM2x}}{4}$. C_{Mf} is the capacitance between source and drain of the filter transistor M_f, and its value is the sum of gate-drain and bulk-drain capacitances, $C_{Mf} = C_{gdMf} + C_{bdMf}$.

The resulting transfer function for the PSR of the proposed voltage reference circuit is shown in equation (14).

$$PSR(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{a_0 + a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2 + b_3 s^3} \tag{14}$$

The coefficients $a_0, a_1, a_2, a_3, b_1, b_2$ and b_3 of the transfer function can be calculated as (15a)-(15g) under the approximations $g_m >> g_o$ and C_{Mf}, C_2 much smaller than the other capacitances in the circuit and where $C_A = C_1 + C_{bd1}$, $C_B = C_{right} + C_{bd1}$ and $G_B = g_{dio} + g_{m3}$.

$$a_0 \approx \frac{g_{o1}G_B + g_{o4}g_{mb1}}{G_{m2}G_B} \tag{15a}$$

$$a_1 \approx \frac{g_{mb1}C_A + G_B C_B}{G_{m2}G_B} \tag{15b}$$

$$a_2 \approx \frac{C_{Mf}(G_B C_B + g_{mb1}C_A)}{g_{of}G_{m2}G_B} \tag{15c}$$

$$a_3 \approx \frac{C_{Mf}(C_B C_{left} + C_A C_{right})}{g_{of}G_{m2}G_B} \tag{15d}$$

$$b_1 \approx \frac{C_f}{g_{of}} \tag{15e}$$

$$b_2 \approx \frac{C_f[G_B(C_2 + C_B) + G_{m2}(C_A + C_{left}) + g_{mb1}C_{bd1}]}{g_{of}G_{m2}G_B} \tag{15f}$$

$$b_3 \approx \frac{C_f[C_{bd1}(C_1 + C_{left}) + C_A C_{right}]}{g_{of}G_{m2}G_B} \tag{15g}$$

In equations (16a)-(16f), the analytical expressions used for the calculation of the PSR parameters are summarized.

$$g_{m3} = \frac{\partial I_{DM3}}{\partial V_{sgM3}} = \frac{I_{DM3}}{n_3 V_T} \tag{16a}$$

$$g_{dio} = \frac{\partial I_{SBM1}}{\partial V_{SBM1}} = \frac{I_{D0}}{n_j V_T} e^{\frac{V_{in}-V_{body}}{n_j V_T}} = \frac{I_{SBM1}}{n_j V_T} \tag{16b}$$

$$g_{mb1} = \frac{\partial I_{DM1}}{\partial V_{SBM1}} = \frac{-\gamma I_{DM1}}{2n_1 V_T \sqrt{2|\Phi_F| + V_{dd} - V_{body}}} \tag{16c}$$

$$G_{m2} = \frac{1}{\sum_{i=1}^{4} \frac{1}{g_{m2i}}} = \frac{1}{4}\frac{\partial I_{DM2}}{\partial V_{sgM2}} = \frac{1}{4}\frac{I_{DM2}}{n_2 V_T} \tag{16d}$$

$$g_{o1,4} \approx \frac{I_{DM1,4}}{V_A} \text{ where } V_A \text{ is Early voltage}^{17} \tag{16e}$$

$$g_{of} \approx \frac{2nV_T \mu_p C_{ox} W_{Mf} e^{\frac{V_{thMf}}{nV_T}}}{L_{Mf}} \tag{16f}$$

Figure 5 shows a comparison of the PSR model developed here, equations (14) and (15a)-(15g), with simulation results using a commercial circuit simulator. The obtained curve using small signal parameters extracted from simulation shows that the developed PSR model offers very good accuracy. The curve obtained using the small signal parameters calculated applying

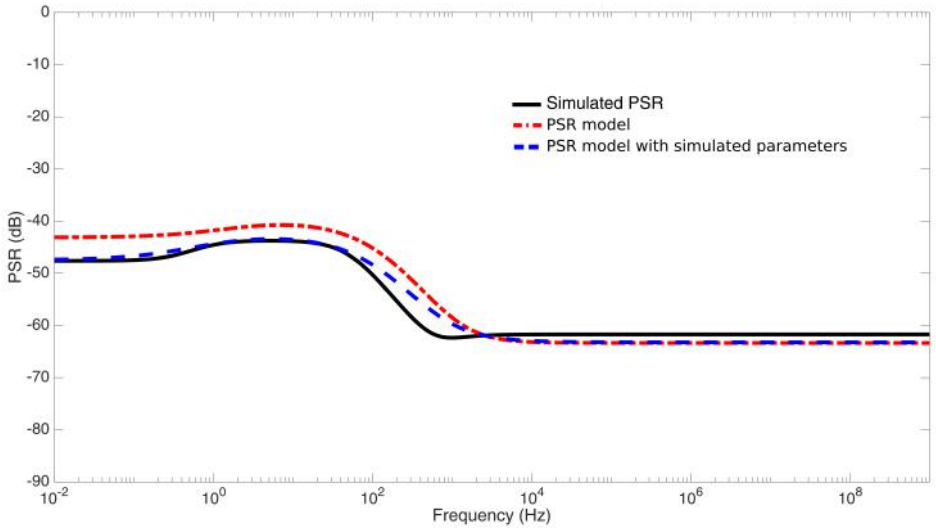


FIGURE 5 Comparison of the analytical PSR model in equation (14) with simulation results.

equations (16a)-(16f) using the current and voltage values determined by the numeric model in section 2.2 provides also a very good estimation of the shape and magnitude of the PSR.

At high frequencies, equation (14) can be simplified as (17). Also, when the M_f transistor is short circuited, the high frequency PSR can be aproximated as equation (18) by solving Kirchhoff equations (13a), (13b), (13c) with $g_{of} \rightarrow \infty$ and $C_{Mf} = 0$. Therefore, the theoretical high frequency PSR improvement due to the incorporation of M_f takes the form of (19). The C_{Mf} capacitor has a small value compared to other parasitic capacitors in the circuit, with a value in the range of fF, while $C_2 + C_{right}$ is in the range of tens of fF. The theoretical PSR improvement calculated with equation (19) is -23.9 dB, while by means of simulation, this improvement has a value of -24.4 dB when a capacitor $C_f = 1.54$ pF is used.

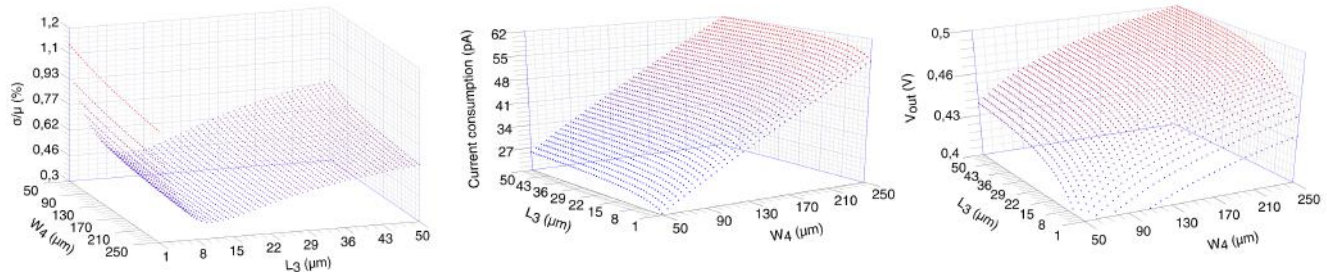
$$PSR_{wM_f f\uparrow\uparrow} = \frac{a_3}{b_3} \approx \frac{C_{Mf}[C_B C_{left} + C_A C_{right}]}{C_f[C_{bd1}(C_1 + C_{left}) + C_A C_{right}]} \tag{17}$$

$$PSR_{w/oM_f f\uparrow\uparrow} \approx \frac{C_{right}(C_A + C_{left}) + C_{bd1} C_{left}}{C_f(C_A + C_{left})} \tag{18}$$

$$\Delta PSR_{f\uparrow\uparrow} = \frac{PSR_{wM_f f\uparrow\uparrow}}{PSR_{w/oM_f f\uparrow\uparrow}} \approx \frac{C_{Mf}(C_A + C_{left})}{C_{right}(C_A + C_{left}) + C_{bd1}(C_1 + C_{left})} \tag{19}$$

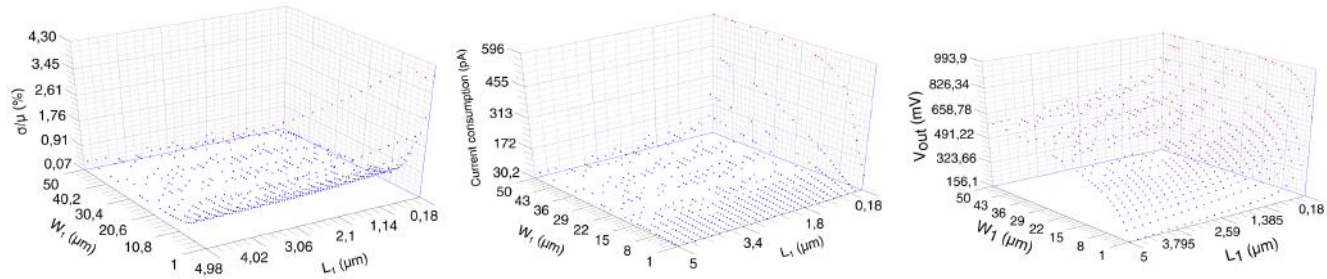
3.3 | Design flow

The design procedure used to determine the transistors sizes was based on parametric Montecarlo simulations, finding the minimum dispersion of voltage V_{out} while keeping the corresponding values for output voltage and current consumption around the intended values. In order to reduce the number of degrees of freedom of the search space, some initial conditions were manually set. Sizes of W/L = 5/5 μm/μm for transistors M_{22}, M_{23} and M_{24} and W/L = 10/5 μm/μm for M_{21} were chosen. These values have been set large enough as to neglect the threshold voltage mismatch between the four transistors. Then, as the aspect ratio of M_4 greatly influences the total circuit consumption and the length of M_3 determines the value of voltage V_{body}, we fixed L_4 and W_3 to 2 μm and performed parametric Montecarlo simulations varying W_4 and L_3. Subsequently, simulations varying only the transistor M_1 geometries were run due to the fact that the aspect ratio of M_1 will determine the current through the right branch of the circuit and the source-bulk current I_{SBM1}. The results of these Montecarlo simulations are shown in Figures 6 and 7 . As it can be seen in Figure 6 , a channel length of M_3 around 15 μm reduces the mismatch and process variations of the output voltage, meanwhile increasing W_4 will reduce dispersion increasing power consumption. Therefore $L_3 = 15$ μm and $W_4 = 150$ μm were chosen as a compromise between dispersion and current consumption. From Figure 7 , a size of 30/5 μm/μm was chosen for transistor M_1 because around these values the output voltage is maximized without having significant consequences on the current consumption.



(a) (b) (c)

FIGURE 6 100 points Montecarlo simulations varying W_4 and L_3: (a) Output voltage dispersion, (b) Mean current consumption, (c) Mean output voltage.



(a) (b) (c)

FIGURE 7 100 points Montecarlo simulations varying W_1 and L_1: (a) Output voltage dispersion, (b) Mean current consumption, (c) Mean output voltage.

TABLE 3 Sizes of all transistors in the fabricated voltage reference circuit proposed in Figure 2 .

Transistor	M_1	M_{21}	M_{22}	M_{23}	M_{24}	M_3	M_4	M_f	M_{S1}	M_{S2}
W/L (μm/μm)	30/5	10/5	5/5	5/5	5/5	2/15	150/2	1/0.6	1/1	1/1

The size of transistor M_f in the passive low-pass filter was fixed equal to 1/0.6 μm/μm because this choice offers good filtering without a significant area increase. The transistors M_{S1} and M_{S2} were manually determined to have an aspect ratio of 1/1 μm/μm. The final selected sizes of all transistors in the circuit are summarized in Table 3 .

The value of the C_f capacitor was chosen as a design compromise between high PSR and reduced silicon area. Figure 8 shows the PSR small signal model evaluation with equation (14) obtained in the previous subsection for various C_f capacitors. As it can be seen, the value used in our simulations, $C_f = 1.54$ pF, represents a good trade-off between PSR improvement and occupied area. The capacitor C_S has a value of 211 fF, high enough to improve the settling time without a significant silicon area increase.

4 | MEASUREMENT RESULTS

The proposed voltage reference circuit was implemented in standard CMOS UMC 180 μm technology. Twenty chips were fabricated, each one including two samples of the proposed circuit. A voltage buffer for each voltage reference was embedded in the chip to avoid loading the circuits under test even if its use increases slightly the dispersion of the measured output voltage.

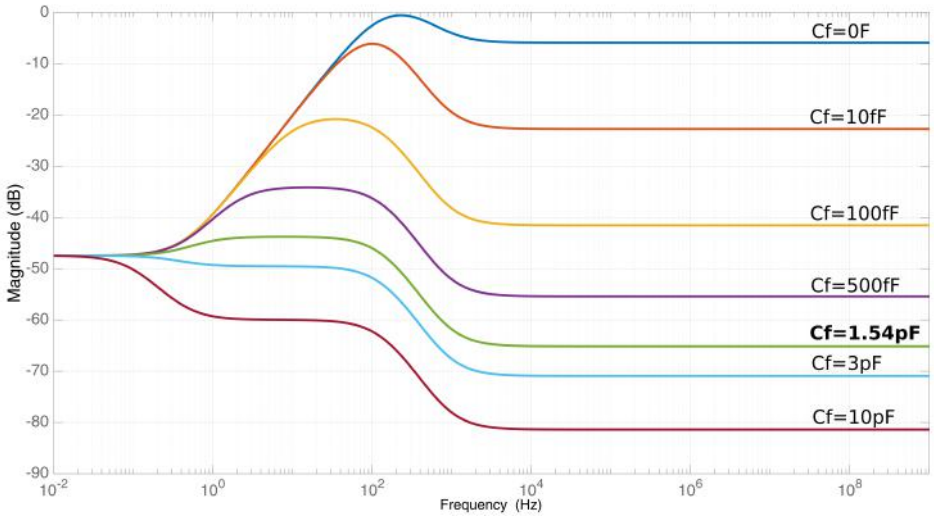
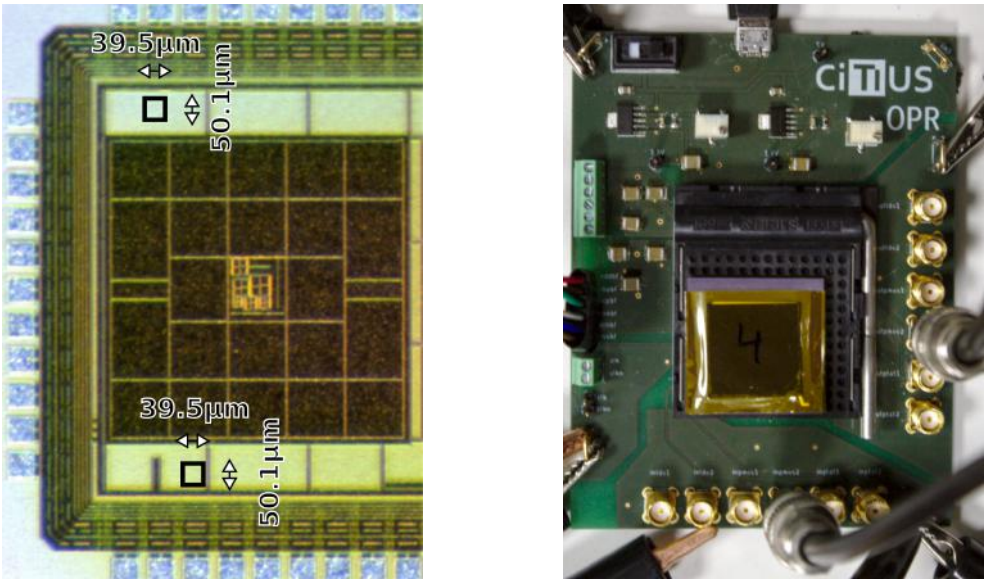


FIGURE 8 Calculated PSR according to equation (14) for various values of capacitor C_f.



(a) **(b)**

FIGURE 9 (a) Chip microphotography with the proposed circuit outer limits marked. (b) Testing PCB photography.

The buffer architecture is based on a conventional structure consisting of a PMOS input differential pair and a folded-cascode summing stage, so that the output reference voltage and the input voltage range of the buffer are compatible.

With respect to the test setup, it consists of a Thermonics T-2650BV as temperature controller, a Tektronix AFG3102C as signal generator, a Keysight MSOX3034A oscilloscope for frequency domain characterization and a Keithley 6485 picoammeter and a Meterman 37XR multimeter for precision current and voltage measurements, respectively. Figure 9 shows a chip microphotography where the positions and the horizontal and vertical dimensions of the two samples of the implemented circuit are highlighted (9 a), and a picture of the test PCB (9 b) used for the experimental characterization presented in this section. The total silicon area occupied by each voltage reference circuit is 1830 μm^2.

Figure 10 plots the measured averaged value over the 40 available samples of the output voltage of the circuit at a temperature of 36 °C as a function of the supply voltage. A mean value of LS = 1.78 %/V was obtained for the line sensitivity when V_{dd} was varied between 0.7 V and 1.8 V. The dispersion of the measured values for both the output reference voltage and the total current

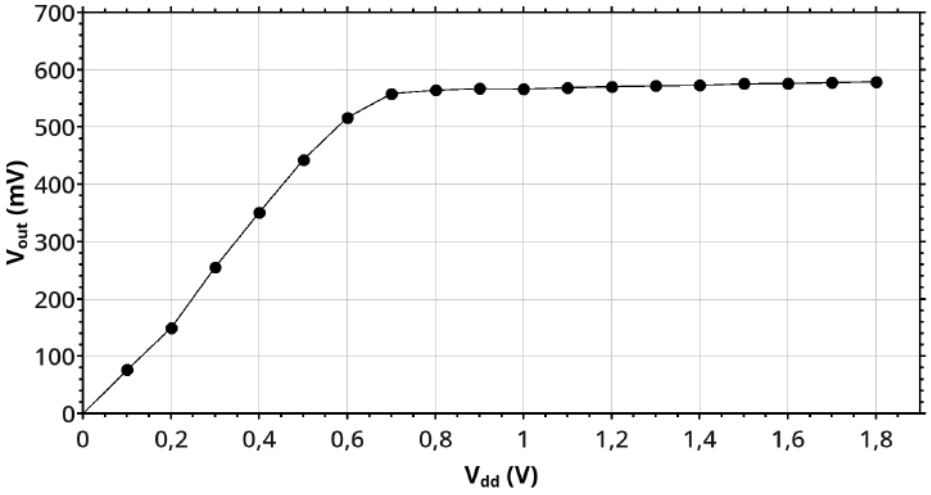


FIGURE 10 Mean measured output voltage of the proposed voltage reference circuit as a function of the supply voltage at a temperature of 36°C.

consumption can be seen in Figure 11 at a temperature of 36°C. As it can be seen, the mean generated reference voltage is $V_{out} = 584.2$ mV, and the dispersion, expressed as a percentage of the mean value, is $\sigma/\mu = 0.65$ %. On the other hand, a mean experimental current consumption of 92.1 pA was obtained, which implies a power consumption at minimum supply voltage $V_{dd} = 0.7$ V of just 64.5 pW.

To assess the robustness of the proposed implementation against supply noise, the measured PSR of the circuit is shown in Figure 12 using a DC supply voltage of 1 V with a superposed sinusoidal signal of 50 mV of amplitude. The measurement of the output voltage amplitude for different frequencies of the sinusoidal input signal was performed using the fast Fourier transform (FFT), calculated by the oscilloscope. As it can be seen, the experimental PSR response over frequency in Figure 12 matches closely the behavior predicted in the previous analysis and simulations, included in Subsection 3.2 and illustrated in Figure 5 . As it may be observed, the obtained PSR is kept below -60 dB from DC up to frequencies of MHz, which demonstrates the robustness of the proposed implementation.

For the sake of completeness, the proposed circuit is compared to state-of-the-art CMOS voltage references in terms of performance in Table 4 . As can be seen, reference [8] achieves the lowest power consumption and silicon area of the comparative, but suffers from a high voltage dispersion with process variations with a σ/μ of 4.9 %. The implementation in [9] has a low power consumption and good PSR, but the generated reference voltage is very low, with a mean value of only 17.69 mV not suitable for many applications, and a line sensitivity greater than 2 %/V. Implementations in [20,21] have very good line sensitivities, with values smaller than 0.1%/V, but power consumption and silicon area are far above other solutions. Besides, they need post-fabrication trimming due to process variation sensitivity. Implementation [6] has a very good power consumption and low V_{out} dispersion before trimming, but makes use of both native transistors and high V_{th} transistors, which are not available in all CMOS technologies. In the case of reference [7], high V_{th} transistors are used and good metrics are obtained, with the best dispersion before trimming found in the comparative.

The proposed implementation offers a good PSR over a wide range of frequencies with low power and acceptable voltage dispersion without trimming. Compared to [13], on which this work was based, the proposed implementation has much lower power consumption with similar PSR but higher line sensitivity. The voltage dispersion values in [13] oscillate between 0.26-0.53 % for the typical and slow wafers compared to the 0.65% of our implementation. Compared to [7], our circuit offers lower power consumption, especially if the power consumption is extrapolated to 36°C. The power consumption of the circuit in [9], on the other hand, has a value of 26.1 pW but with a supply voltage of 150 mV and 25 °C of temperature, which implies a current consumption of 174 pA compared to the 92.1 pA consumed by our solution with a supply voltage of 0.7 V. Finally, the implementation in [6] offers very good metrics but requires types of transistors not available in all CMOS technologies, whereas the implementation proposed in this paper is compatible with standard CMOS technology.

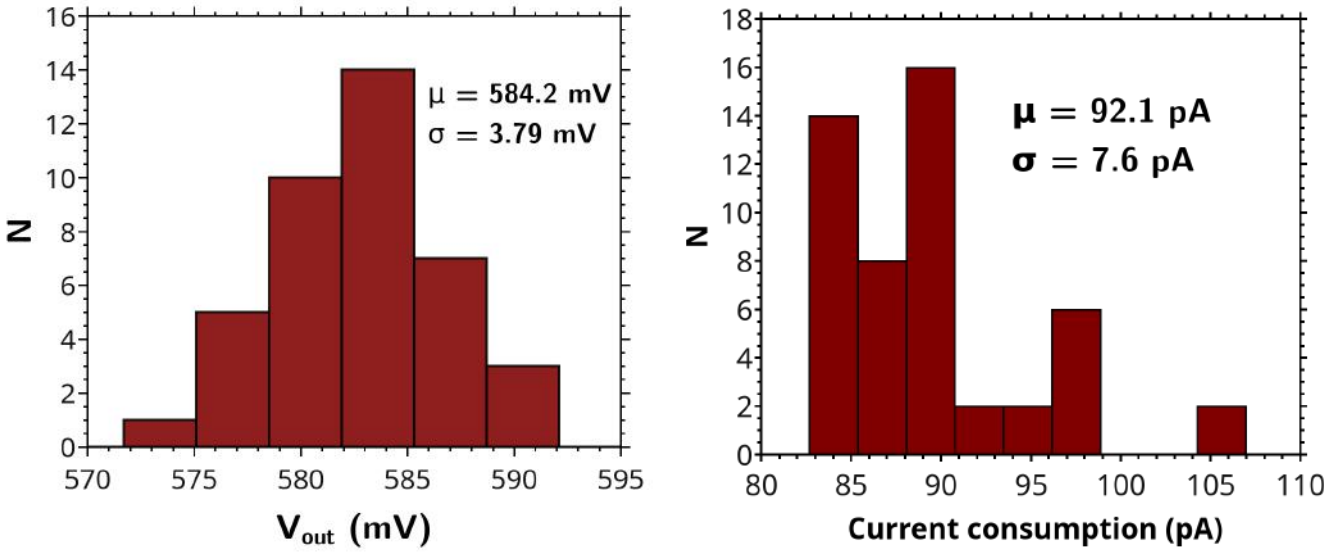


FIGURE 11 Measured values distributions of (a) output reference voltage and (b) current consumption of the proposed voltage reference circuit.

TABLE 4 Comparison of the proposed voltage reference with state-of-the-art.

	This work	Dong[13]	Lee[6]	Wang[8]	Alhassan[20]	Albano[9]	Campos[7a]	Liu[21]
Process	0.18 μm	0.18 μm	0.18 μm	65 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Supply (V)	0.7-1.8	1.2-	1.4-3.6	0.4-	0.8-2.2	0.15-1.8	0.45-3.3	0.4-
Power (pW)	64.5	114	35	0.42	360000	26.1	54.8	9600
@ V_{dd}(V)	0.7	1.2	1.4	0.4	0.8	0.15	0.45	0.4
@ T (°C)	36	25	27	27	27	25	27	27
V_{out} (mV)	584.2	986.2	1250	342.8	489	17.69	225.3	210
$(\sigma/\mu)_{V_{out}}$(%)	0.65	0.26|0.53⋆	0.81 | 0.27‡	4.9	1.9 | 0.5‡	1.6	0.63	1.48 | 0.31‡
LS(%/V)	1.78	0.38	0.31	0.47	0.076	2.03	0.15	0.027
PSR (dB)								
@100Hz	-61	-42	-41	-	-75	-64	-43.9	-47
@10MHz	-62	-56	-	-	-59	-124†	-	-
Area (μm^2)	1830	4880	2500	104	18000	1200	2000	16000

†Simulation results.
‡Trimmed dispersion.
⋆0.26% for the "Typical Wafer" and 0.53% for the "Slow Wafer".
[a]In[7] two implementations are proposed, and the one with the lowest consumption is shown in the table.

5 | CONCLUSIONS

A voltage reference circuit for implantable devices, based on a PMOS-only V_{ref} core section, was designed with focus on reduced power consumption and robustness to mismatch and process variations. Moreover, a precise mathematical model was proposed for the accurate estimation of the output voltage generated by the voltage reference core, taking into account transistors' body

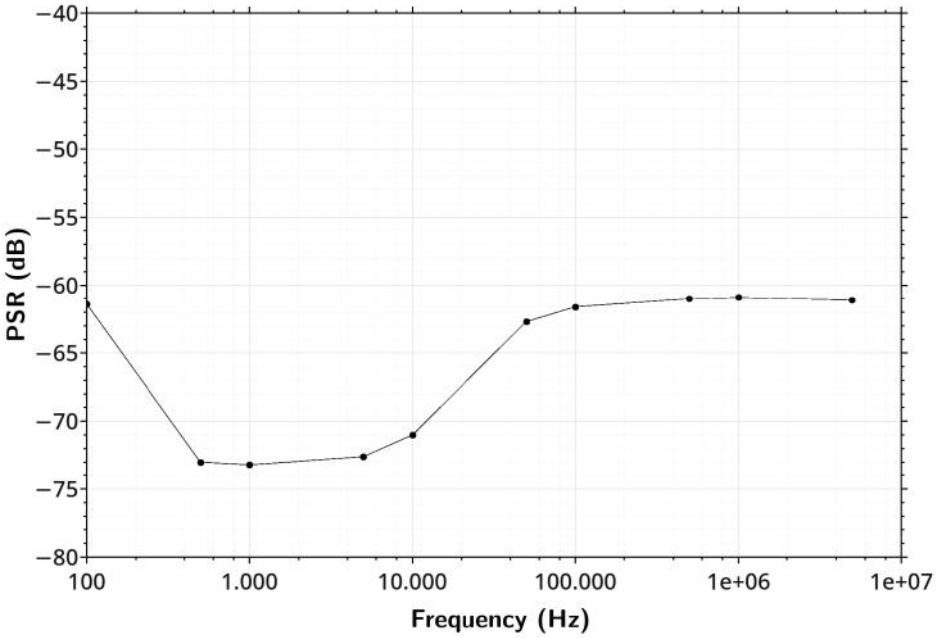


FIGURE 12 Measured PSR vs frequency with a DC supply voltage of 1 V.

effect and threshold voltage dependency with W and L. A numerical solution of the model was derived showing excellent agreement when compared to extensive electrical simulations. Then, a PSR analysis, based on a small-signal model, was performed to predict the rejection of the circuit to supply noise. A silicon prototype was fabricated in UMC standard 0.18 μm CMOS technology. The average power consumption was experimentally determined to be equal to only 64.5 pW at a supply voltage of 0.7 V and a trimming-free dispersion of the reference output voltage equal to $\sigma/\mu = 0.65$ % was measured giving a mean output voltage of 584.2 mV. The average PSR was found to be below -60 dB over a frequency domain from DC up to the MHz range. Therefore, the proposed design methodology represents a suitable approach to implement an ultra-low power trim-free voltage reference for body implantable electronic devices.

ACKNOWLEDGMENTS

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