Design methodology of a 0.7 V, 64.5 pW @ 36ºC, 1830 μm^2 Subthreshold Voltage Reference for Implantable Devices

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***Abstract*—A picowatt CMOS voltage reference for body implantable devices is presented in this paper. The circuit is based on a PMOS-only voltage reference core with a passive RC filter to enhance the supply noise rejection and a speed-up mechanism to improve the switching-on time of the circuit. The measured power consumption at a supply voltage of 0.7 V is as low as 64.5 pW at the reference human body temperature of 36 ºC, with a PSR better than -60 dB until frequencies of MHz.**

I. Introduction

Voltage references are basic components in many analog circuits such as amplifier's biasing blocks, voltage regulators or analog to digital converters and are usually an always-on part of the system. In power-constrained applications such as wearables, biomedical implantable devices or autonomous Internet of Things (IoT) nodes, it is essential to reduce consumption, especially in those parts of the system that are continuously working.

In CMOS technology, to achieve ultra-low power consumption, transistors in the weak inversion working-regime can be used for voltage reference implementation. Different approaches can be found in the literature which can be roughly classified as based on different threshold voltage transistors [1]–[5] or on different current densities [6]–[9]. The former usually achieve very low power consumption and good power supply rejection (PSR) and line sensitivity (LS) but are sensitive to process variations due to the explicit dependence of the output voltage with the threshold voltages, being necessary post-fabrication trimming to reduce reference voltage dispersion. Furthermore, some of these proposals [1], [3] use various types of transistors to generate the different threshold voltages, which imply additional manufacturing steps and therefore more process variations.

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In the latter, on the other hand [6]–[8], [10], the gate-source voltage differences originated by a current flowing through transistors with different W/L ratio [11] or by different drain currents are used to generate the reference voltage, resulting in a proportional to absolute temperature (PTAT) voltage. On first approximation, they are not threshold voltage-dependent but have a large temperature coefficient, and if a wide temperature working range is required, a complementary to absolute temperature (CTAT) compensation circuit must be appended, resulting in higher area and power consumption.

In [12] a voltage reference circuit built only with PMOS transistors is presented, in which the output voltage is obtained from threshold voltage modulation by source-body biasing. The generated reference voltage by this mechanism is approximately threshold-voltage-independent and has low sensitivity to process variations. Therefore, with proper transistor sizing, it is possible to achieve temperature compensation.

In this contribution, the design methodology of a reference voltage for implantable devices is described. The design constraints, in this case, are ultra-low power consumption maintaining small form-factor while other metrics such as the temperature dependence are of minor relevance. The proposed implementation is based on contribution [12] and uses only regular threshold voltage transistors. Experimental results in UMC 180 nm technology, show a total power consumption equal to 64.5 pW using a supply voltage of 0.7 V and at 36 ºC of temperature. The proposed solution has a total layout area of 1830 μm^2, a measured PSR below -60 dB up to a frequency of 10 MHz and an output voltage dispersion $\sigma/\mu = 0.65$ %.

II. Proposed voltage reference circuit

We take as baseline the voltage reference structure illustrated in Fig. 1. The core of the circuit is based on the PMOS-only voltage reference introduced in [12]. Nevertheless, our design has been particularized to the context of an implantable device, where ultra-low power consumption is mandatory. Besides, a chain of four diode connected transistors M_{2x} is

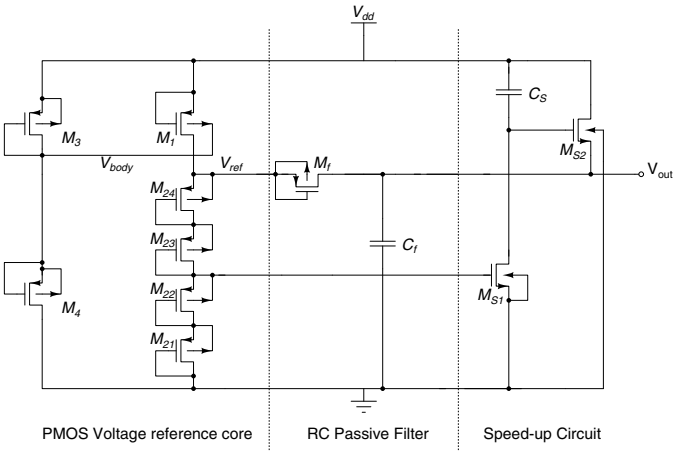


Fig. 1. Circuit schematic of the proposed voltage reference.

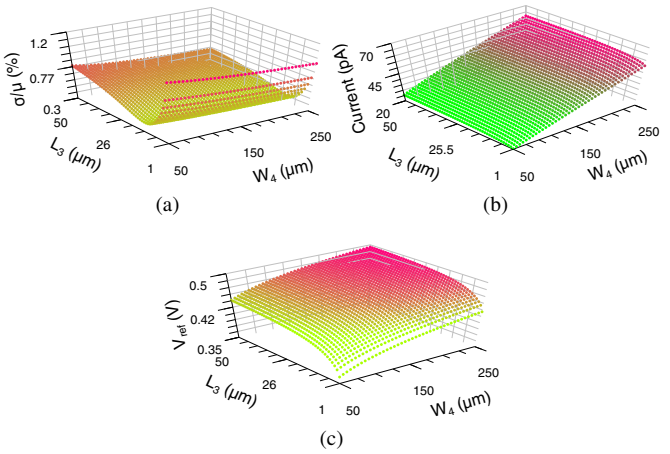


Fig. 2. 100 points Montecarlo simulations varying W_4 and L_3: (a) dispersion of the output voltage, (b) average current consumption, (c) average reference voltage.

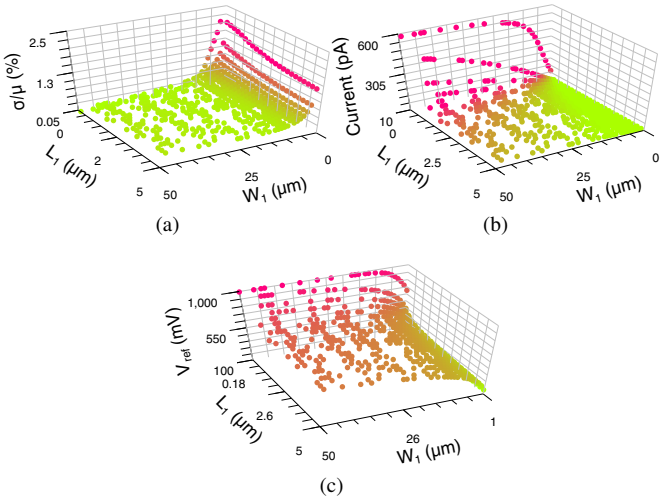


Fig. 3. 100 points Montecarlo simulations varying W_1 and L_1: (a) dispersion of the output voltage, (b) average current consumption, (c) average reference voltage.

used, instead of only one device, in order to achieve higher reference voltages without increasing the current flowing through transistor M_1. Our solution features as well an RC passive filter to improve PSR and a speed-up circuit. The design flow of these blocks is described in detail in Section III.

III. Design Methodology

The first step in the design procedure of the circuit was to determine the appropriate aspect ratios of the transistors in the PMOS voltage reference core in Fig. 1. The design constraint was to ensure a total current consumption below 100 pA while keeping a low output voltage dispersion in V_{ref} at the desired operating temperature of 36 °C. To achieve this, parametric Montecarlo simulations were performed using a commercial circuit simulator. To reduce the search space region, some initial transistors' aspect ratios were manually determined, such as the W/L of M_{21}, M_{22}, M_{23} and M_{24}, the width of M_3, W_3, and the length of M_4, L_4. Figures 2 and 3 show the simulation results sweeping W_4, L_3 and W_1, L_1, respectively. Based on these Montecarlo simulations, a value of L_3 = 15 μm was chosen as it minimizes dispersion, whereas for the width of M_4, a value of W_4 = 150 μm was selected because it offers a low current consumption without decreasing the output voltage significantly. From Fig. 3, the final values chosen for W_1/L_1 were 30/5 μm/μm, offering acceptable dispersion, current consumption and output voltage.

In addition to the voltage reference core, our solution includes a cut-off transistor, M_f, that together with the capacitor C_f act as a passive RC filter to improve the high frequency PSR. Electrical circuit simulations show that the actual dimensions of transistor M_f do not have a significant impact on the PSR and therefore, a compromise value of 1/0.6 μm/μm was chosen to minimize area consumption. To determine the value of C_f, the small signal model of the circuit was evaluated varying the capacitance value while maintaining M_f fixed. A value of $C_f = 1.54$ pF was finally chosen as a good trade-off between power supply rejection and area consumption as it can be seen in Fig. 4. Using this capacitor value, electrical simulations shown that the RC filter formed by M_f and C_f results in a PSR improvement of 24 dB at high frequencies compared to the use of the capacitor alone.

On the other hand, the speed-up mechanism is constituted by the transistors M_{S1} and M_{S2} and the capacitor C_S. Its function is to reduce the switching-on time of the circuit as the very low current flowing through each branch together with the high impedance of the cut-off transistor M_f would otherwise result in a large time to charge the filter capacitor and then set the output voltage. When the supply voltage suddenly changes from 0 to V_{dd}, the voltage at the gate of M_{S2} will be closer to V_{dd}, and then a certain current will flow across M_{S2}, charging the capacitor C_f and rapidly increasing the output voltage. The voltage at the gate of M_{S2} will be decreasing due to the current across M_{S2}, isolating the input and the output node. The capacitance of C_S in conjunction with the aspect

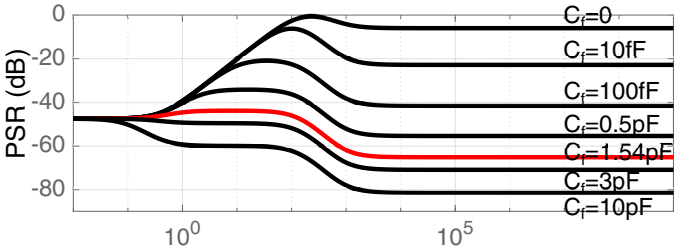


Fig. 4. PSR calculation for various C_f values.

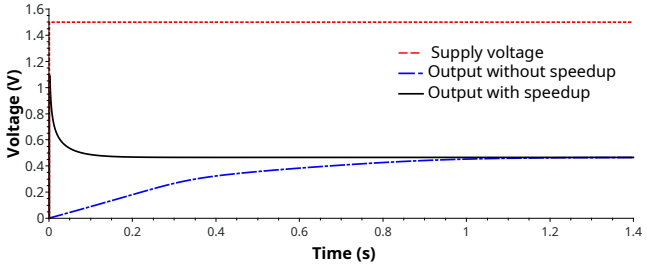


Fig. 5. Simulated switching on time with and without speed-up circuit.

TABLE I
ASPECT RATIOS OF TRANSISTORS IN THE CIRCUIT IN FIG. 1.

Device	Size
M_1	30/5 μm/μm
M_{21}, M_{23}, M_{24}	10/5 μm/μm
M_3	2/15 μm/μm
M_4	150/2 μm/μm
M_f	1/0.6 μm/μm
M_{S1}, M_{S2}	1/1 μm/μm
C_S	211 fF
C_f	1.54 pF

ratio of M_{S2} will affect the conduction time of M_{S2} in a transient state. Based on circuit simulations, M_{S1} and M_{S2} were manually set equal with channel dimensions 1/1 μm/μm, and a value of C_S = 211 fF was selected as a good trade-off between speed-up and silicon area consumption. Under this approach, the switching-on time improvement of the speed-up circuit is shown in Fig. 5 for an abrupt change of the supply voltage from 0 to 1.5 V. As observed, the 2% settling time, in this case, shows a $\times$10 improvement going from 1.06 s to 100 ms compared to not using the speed-up circuit.

Table I includes the sizes of all the devices integrating the voltage reference circuit which was implemented in silicon. With the chosen device parameters, the expected value for the output voltage determined by simulation is 469 mV, with a current consumption of only 36 pA at a minimum supply voltage of 0.7 V, as it can be seen in Figs. 6 and 7. Besides, a line sensitivity of 0.68 %/V and a PSR below -45 dB are obtained with the electrical simulator.

IV. EXPERIMENTAL RESULTS

Twenty five chips containing two samples of the proposed circuit were fabricated in UMC 0.18 μm. Each circuit has a PMOS input pair folded-cascode buffer connected to its output to avoid loading the circuit with the chip pads and the measurement instrumentation.

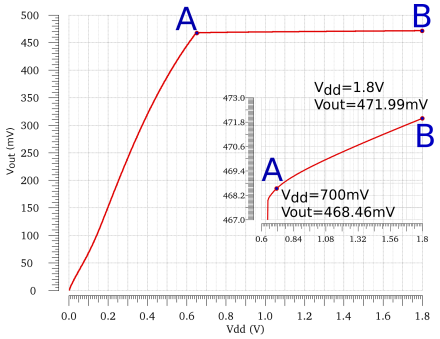
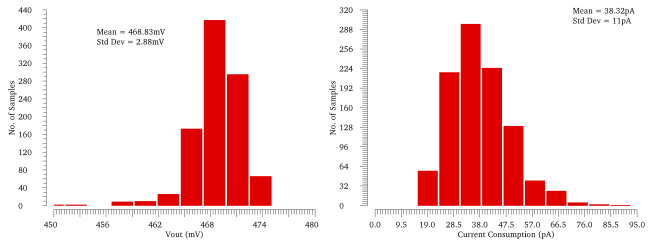


Fig. 6. Simulated output voltage as a function of the supply voltage.



(a) (b)

Fig. 7. Output voltage (a) and current consumption (b) histograms obtained with Montecarlo simulations.

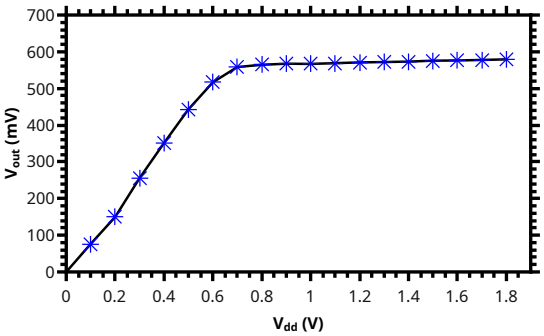
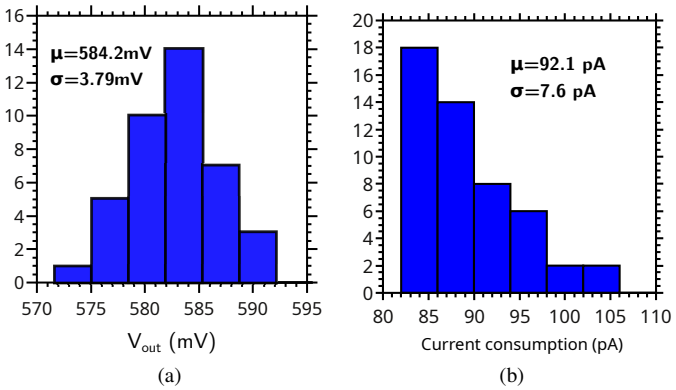


Fig. 8. Average value of the output voltage over the supply voltage for T = 36 °C.

Fig. 8 shows the experimental output voltage variation with the supply voltage V_{dd}. From the obtained data, an experimental mean line sensitivity of LS = 1.78 %/V can be calculated when the supply voltage is varied from 0.7 V to 1.8 V. In Fig. 9a, the measured histogram of the output voltage is shown, from where a mean value of 584.2 mV is obtained with a dispersion $\sigma/\mu = 0.65\%$. This experimental value of the reference voltage is larger than the simulated result of 469 mV. This variation is in line with previously published data as in [3]. A similar trend is observed for the current consumption distribution of the measured samples shown in Fig. 9b, with a mean value of 92.1 pA at the minimum supply voltage of 0.7 V, equivalent to an average power consumption of 64.5 pW.



(a) (b)

Fig. 9. Histograms of measured data distributions: (a) Output voltage (b) Current consumption.

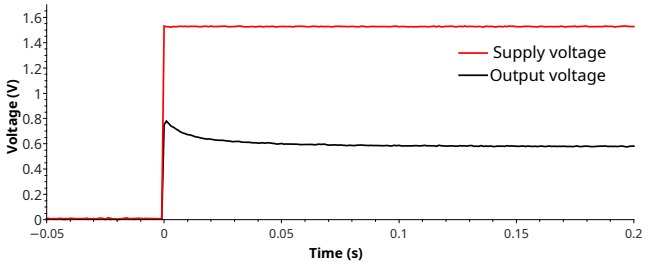


Fig. 10. Experimental average time response of the circuit at T = 36 °C when the supply voltage goes from 0 to 1.5 V .

Fig. 10 shows the experimental average transient response of the circuit when the supply voltage suddenly changes from 0 to 1.5 V, obtaining an experimental 2% settling time of 62 ms, which is even faster than the simulated time of 100 ms in Fig. 5.

The mean measured PSR values can be seen in the Fig. 11, from where values better than -60 dB are obtained until frequencies in the MHz range.

Making a comparison with state-of-the-art voltage references, the solution introduced offers good power consumption and PSR with moderate silicon area. The voltage reference proposed in [4] offers a very reduced power consumption, as low as 420 fW, and a small layout area of only 102 μm^2, but displays a high voltage dispersion of $\sigma/\mu = 4.9$ %. The

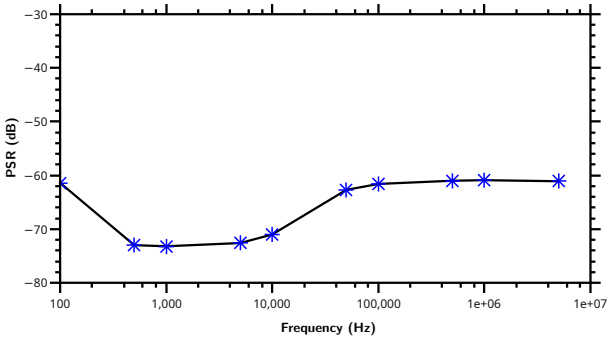


Fig. 11. Average measured PSR for a supply voltage of 1 V.

implementation shown in [5] offers better power consumption and PSR than our solution, but the output voltage has a value of 17.69 mV, too low for most applications, and a line sensitivity above 2 %/V. Implementations in [8], [9] offer very good line sensitivities smaller than 0.1 %/V, but occupied area and power consumption are significantly higher. Compared with [12] in where the PMOS-only voltage reference core was introduced, the proposed circuit offers a lower power consumption with similar PSR and higher line sensitivity.

V. Conclusion

In this paper the design methodology for ultra-low power consumption of a voltage reference based on a PMOS-only core is proposed. The complete circuit has been designed and fabricated in standard 0.18 μm CMOS technology for operation at supply voltages between 0.7 V and 1.8 V. Experimental results are provided, showing a mean output reference voltage of 584.2 mV with an average power dissipation equal to 64.5 pW when the circuit is fed with a supply voltage of 0.7 V at the human body reference temperature of 36° C.

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