ResearchGate

See discussions, stats, and author profiles for this publication at: https://www.researchgate.net/publication/314224208

Fluctuation Sensitivity Map: A Novel Technique to Characterise and Predict Device Behaviour Under Metal Grain...

Article *in* IEEE Transactions on Electron Devices · March 2017

DOI: 10.1109/TED.2017.2670060

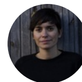
CITATIONS
0

READS
11

4 authors, including:

Guillermo Indalecio
University of Santiago de Compostela
24 PUBLICATIONS **65** CITATIONS

SEE PROFILE

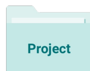

Natalia Seoane
University of Santiago de Compostela
73 PUBLICATIONS **575** CITATIONS

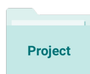
SEE PROFILE

Antonio Garcia Loureiro
University of Santiago de Compostela
166 PUBLICATIONS **678** CITATIONS

SEE PROFILE

Some of the authors of this publication are also working on these related projects:


Thesis View project


Adaptive High-Performance I/O Systems View project

All content following this page was uploaded by Guillermo Indalecio on 02 May 2017.

The user has requested enhancement of the downloaded file. All in-text references underlined in blue are added to the original document and are linked to publications on ResearchGate, letting you access and read them immediately.

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

Fluctuation Sensitivity Map: A Novel Technique to Characterise and Predict Device Behaviour Under Metal Grain Work-Function Variability Effects

G. Indalecio, N. Seoane, K. Kalna and A. J. García-Loureiro

***Abstract*—A new technique developed for the analysis of intrinsic sources of variability affecting performance of semiconductor devices is presented. It is based on the creation of a Fluctuation Sensitivity Map (FSM), which supplies spatial information about the source of variability affecting the device performance and reliability, providing useful advice in the development of fluctuation-resistant device architectures. We have applied the FSM to metal grain work-function variations (MGWV), since they are one of the major contributors to device variability. This technique is computationally very efficient because, once the original FSM is created, it can be used to predict the MGWV for different metal gates or grain sizes. Two state-of-the-art devices were used as test-models: a 10.7 nm gate length Si FinFET and 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET. The cross-section shape (triangular, rectangular or bullet), the metal used in the gate (TiN or WN), and the grain size (10, 7 and 5 nm) have been used as test scenarios for this technique.**

***Index Terms*—Intrinsic parameter fluctuations, Voronoi, gate work function variability, sensitivity map, FinFETs.**

I. Introduction

Variability in performance of nanoscale semiconductor transistors plays an essential role to determine viability of the particular technology solution in circuit operations [1]. Variations in device performance induced by metal grain work-function (MGW) [2], [3], line-edge roughness (LER) [4], [5], or random dopant fluctuations (RDF) [6], [7] become the most critical at nanoscale dimensions [8]. Computational evaluation of variations requires demanding statistical analysis of a large ensemble of 3D specimens of the technology solution. A study of variability in the sub-threshold region, dominated by electrostatic, can be carried out by a relatively fast approach like quantum corrected drift-diffusion simulations [9], but a study in the on-region needs more complex 3D techniques [11], like ensemble Monte Carlo [10] or Non-Equilibrium Green Functions [7], which increases the computational time. A majority of these statistical studies are relatively simple and use the standard deviation (σ) (or other purely statistical parameters) as the main criteria for analysis. These parameters do not account for any type of information related to the location of the fluctuations and, therefore, the information they provide will be incomplete, lacking the insight necessary to comprehend how the different regions of a device contribute to the variability. For the RDF, the spatial dependence of the correlation between an uncertain parameter and device variability has been explored [12] by defining a statistically significant region in the device where the impact of the dopants was the largest. Moreover, the Impedance Field Method [13] was developed again for the RDF to obtain the effect of small perturbations in the device without having to actually simulate the device for each variability scenario, as long as both the perturbations and their effect were relatively small.

In this paper, we present a new approach to evaluate the sensitivity of different regions of the gate of a semiconductor device to the MGW variability (MGWV). This technique, which is based on the creation of a Fluctuation Sensitivity Map (FSM), will provide i) useful spatial information about the effect of variability on the device performance and ii) a prediction of the magnitude of the variability for a particular figure of merit (FoM). Therefore, this approach, which obtains simulation results at a reduced time, can be beneficial in the design of fluctuation-resistant architectures of semiconductor devices.

The structure of the paper is as follows. Section II describes how the fluctuation sensitivity maps are created. Section III presents different case studies where the FSM may be useful. Section IV explains how the FSM can be used to predict the standard deviation of the MGWV for a FoM. The conclusions are drawn up in Section V.

This work is supported by Spanish Government (TIN2016-76373-P), by the Consellería de Cultura, Educación e Ordenación Universitaria (accreditation 2016-2019, ED431G/08), the European Regional Development Fund (ERDF), and Xunta de Galicia (project GRC 2014/008). NS received funding from the Spanish Ministry of Economy and Competitiveness (TEC2014-59402-JIN) and FEDER. GI, NS, and AGL are with the CITIUS, University of Santiago de Compostela, Spain. KK is with the Nanoelectronic Devices Computational Group, College of Engineering, Swansea University, United Kingdom. E-mail: (guillermo.indalecio@usc.es).

II. Construction of the FSM

A map is constructed with the aim to represent the sensitivity to the fluctuations in the different regions of the metal gate using a $M \times N$ matrix named FSM. In this case the map is two dimensional because the region of interest is the gate contact. The elements of this matrix ($FSM_{i,j}$) are mapped to points (u, v) of the metal gate (see Fig. 1) which has been uniformly discretised by $M \times N$ elements. The value of an element $FSM_{i,j}$ will represent how sensitive a certain FoM is to the grain orientation at the position in the gate. Low values represent a low sensitivity, so the FoM will be changing negligibly with the grain orientation at that position of the gate. High values of the FSM (positive or negative) will represent a high sensitivity, so the FoM is changing significantly when the grain orientation at that point changes. The construction of the FSM can be mathematically expressed as follows:

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

Let us consider the function $f:(i,j)\rightarrow(u,v)$ that maps the indices of the FSM matrix to points in the gate of the device. Let $WF^k(u,v)$ be the work-function value at a point (u,v) of the gate for the k-th device configuration, and ϕ^k the resulting value of a certain FoM when this configuration is simulated. With this notation, the local sensitivity can be expressed for each of the simulations as:

$$FSM^k_{i,j} = \frac{\partial \phi^k}{\partial WF^k(f(i,j))} \tag{1}$$

If P is the total number of device configurations, we minimise the residual of this equation by fitting $a(i,j)$ and $b(i,j)$, for each node location (i,j) as:

$$\phi^k - \Big(a(i,j) + b(i,j)\cdot WF^k(f(i,j))\Big) = 0 \quad \forall k\in[1,P] \tag{2}$$

Finally, the value of each element of the matrix $FSM_{i,j}$ (see Eq. 1) will be the slope of the linear fit as:

$$FSM_{i,j} = b(i,j). \tag{3}$$

A detail explanation of how to use this constructed FSM to predict the MGWV can be found in Section IV.

III. Case studies

As a particular example, we have chosen state-of-the-art nanoscale FinFETs as test devices to prove the validity of this approach. Note that a similar study can be done for other device architectures (e.g. nanowire FETs, double-gate FETs, etc.).

We investigate two channel materials (Si and $In_{0.53}Ga_{0.47}As$) and four cross-section shapes which have been accurately described via finite elements. Following the appropriate scaling of experimental transistors [14], [15], we have modelled three multigate devices, two of them with a rectangular-shaped channel and either a relatively thin top oxide, as illustrated in Fig. 2(a) (REC-Thin), or a more realistic triangular-liked top oxide (originating from etching process), as seen in Fig. 2(b) (REC). The third device has a bullet-shaped channel (BUL) as shown in Fig. 2(c). Moreover, for comparison purposes, the triangular-shaped channel device in Fig. 2(d) has been selected as an extreme case resulting from etching process [16]. Note that the body of the device has rounded corners in all the analysed structures accurately described by a finite element mesh. All the simulated transistor structures have been designed following the ITRS specification [17] and have the same: i) gate length (10.4/10.7 nm for InGaAs/Si), ii) fin width (6.1/5.8 nm for InGaAs/Si) and iii) cross-sectional area (93/87 nm^2 for InGaAs/Si) but different fin heights.

Initially, in order to create the FSM, two inputs are needed: i) the distribution of WF values over the device gate for each simulated device configuration, and ii) the value of the FoM (e.g. V_T, SS, I_{OFF}, I_{ON}) that such WF distribution produces. Two metal gates have been considered: i) TiN, which has two

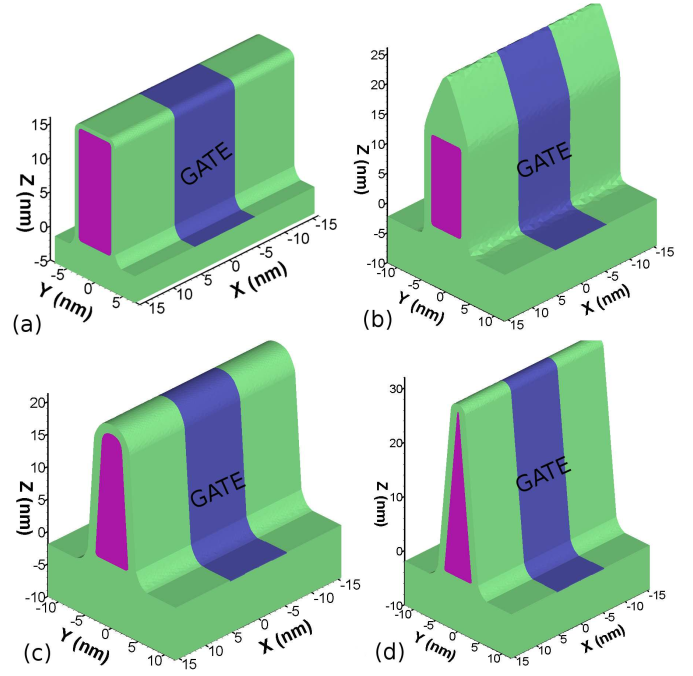


Fig. 2. Schematic structure of the FinFET architectures investigated: a) rectangular-shaped channel with a thin oxide buffer on the top of a gate (REC-Thin), b) rectangular-shaped channel with a thick oxide buffer (of 11.0 nm) on top of the gate (REC), c) bullet-shaped channel (BUL), and d) triangular-shaped channel (TRI). All the devices are described by a finite element mesh with rounded corners in the body.

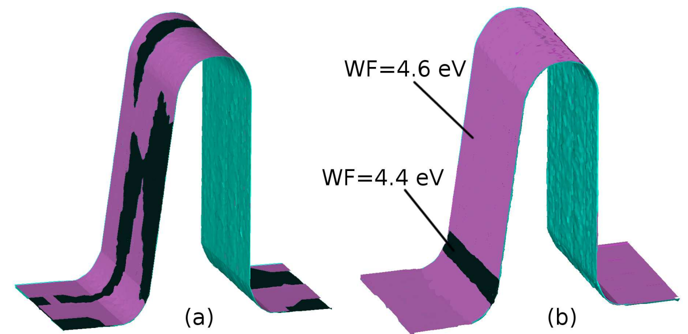


Fig. 3. Two examples of a MGW profile applied to the gate of a bullet-shaped channel FinFET: (a) shows a Voronoi generated grain distribution (with $GS = 5$ nm) for a TiN metal gate, and (b) shows a synthetic profile in which the gate has a constant work-function $WF = 4.6$ eV, apart from a small horizontal strip where $WF = 4.4$ eV.

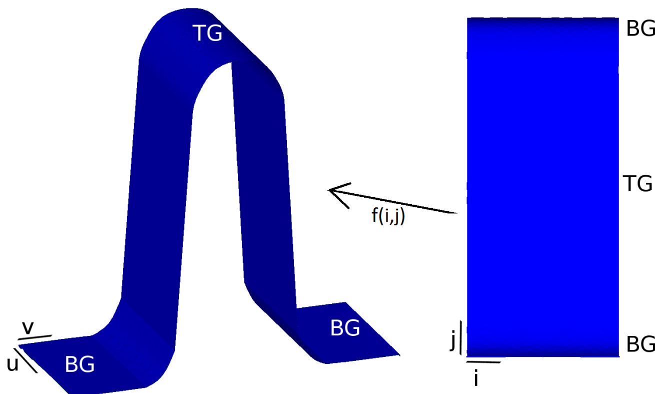


Fig. 1. Example of the mapping of points (u,v) in the metal gate of a semiconductor transistor to a 2D structure of dimensions $M\times N$ with indices (i,j). The top of the gate (TG) and bottom of the gate (BG) are indicated.

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

possible orientations of the grains with WF values of 4.6 and 4.4 eV and probability of occurrence 60% and 40%, respectively, and ii) WN, which has four possible grain orientations with WF values of 4.5, 4.6, 5.3 and 4.2 eV and probability of occurrence 65%, 15%, 15% and 5%, respectively [18]. As we mention in the previous section, both the FSM and the gate are characterised via a 2D matrix that, in this case, has a 100×200 dimension. The distribution of WF along the gate has been modelled using Voronoi diagrams [19], [20], which provides a realistic physical representation of the grains that compose the gate [21].

For each FinFET, ensembles of 300 devices were generated, each with a different gate WF distribution (see an example in Fig. 3a for an average grain size (GS) of 5 nm), and simulated in order to extract the main FoMs that characterise each individual device. These simulations have been done with two in-house built 3D finite-element (FE) density-gradient (DG) quantum-corrected tools: i) a drift-diffusion (DD) simulator [22] (that was previously calibrated against Silvaco's [23] NEGF simulations [24]) for off-region studies, and ii) a Monte Carlo (MC) simulator [25] in the on-region.

A. Impact of the Device Geometry

A V_T MGWV study performed for the four previously described cross-section shapes has given the V_T standard deviation of the distributions around 32 mV independently of the cross-section shape, with maximum differences of 5% only indicating a good immunity of the MGW variability to the cross-section shape [26]. Therefore, if we limit the study to a comparison of the σ of the distributions, we will be missing important information about the devices behaviour. For instance, Fig. 4 shows the 2D threshold voltage fluctuation sensitivity maps for the four analysed cross-section shapes that provide visual information of how sensitive the V_T of a device is to the WF present in the different regions of the gate. Note that the lighter the colour, the more sensitive a region of the gate is to the MGWV. The sensitivity is expressed in mV/eV, with the MGWV in eV and the FoM (V_T) in mV. The top (TG) and bottom (BG) of the gate are indicated as defined in Fig.1 together with the middle gate (MG), the source/gate (SG) and drain/gate (DG) ends. In the REC-Thin and BUL devices, the top and sidewalls of the gate are the most sensitive regions to the WF variations because the high electron density is concentrated at the top of the cross-section, as seen in [26]. In the REC device, there is a thick layer (of 11 nm) of oxide over the channel (a relict of etch process), which reduces the impact on the device V_T by any metal grain placed on the top of the gate region. Therefore, for the REC device, the FSM shows that the grains present in the sidewall region of the gate are the most influential. When analysing the FSM for the TRI device, we observe that the region that spans from the bottom to the sidewalls of the gate is the most sensitive to the MGW variations. Note that, for this device, the high electron density is mostly located at the bottom of the cross-section, where the channel widens, and is low at the narrow top due to stronger quantum mechanical confinement [16], [26].

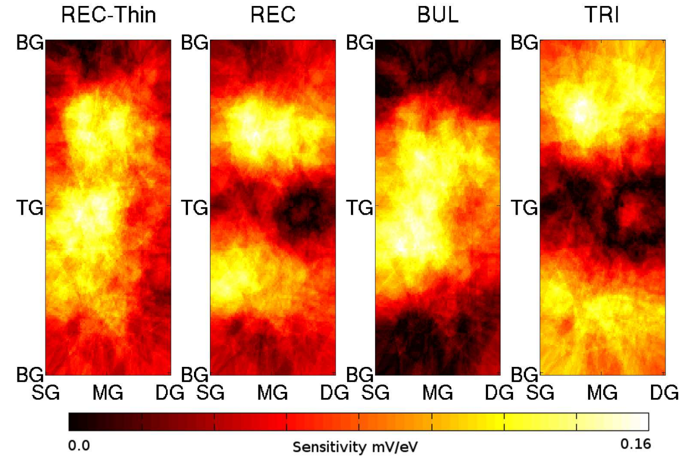


Fig. 4. 2D V_T FSMs for the four cross-section shapes of $In_{0.53}Ga_{0.47}As$ FinFETs at V_D=0.05 V. The grain size is 7 nm.

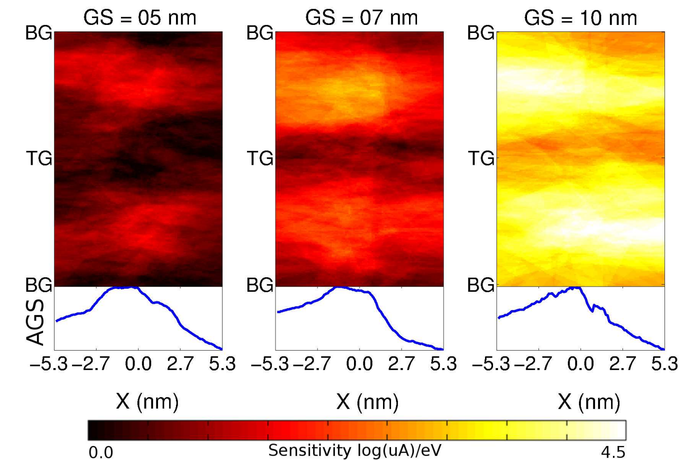


Fig. 5. 2D I_{off} FSMs for the rectangular (REC) cross-section shape Si FinFET at V_D=0.05 V as a function of the grain size (top) and 1D aggregated gate sensitivity (AGS) along the transport direction (bottom).

B. Impact of the Grain Size

We have analysed the effect that the average grain size (GS) of the grains that compose the gate has on the off-current (I_{OFF}) and the on-current (I_{ON}) using the FSM. This study has been done for the rectangular (REC) cross-section shape FinFETs. Figs. 5 and 6 show, respectively, the 2D off- and on-current fluctuation sensitivity maps for grain sizes of 5, 7 and 10 nm. As already seen in Fig. 4, the sidewalls of the gate are the most sensitive regions to the MGWV. The I_{OFF} FSM shows that, independently of the grain size, the grains that occupy the middle of the gate and its proximity are dominant contributors to the variability. In order to demonstrate this, we define the 1D aggregated gate sensitivity (AGS) for a particular X coordinate, as the addition of all the FoM values that compose the column of the FSM associated to that coordinate, which is then normalised to a value between 0 and 1. The AGS along the transport direction (X) is shown at the bottom plots of Fig. 5, where it can be seen that the sensitivity concentrates at the middle of the device. In the case of the I_{ON}, the FSM shows that the sensitivity is much larger at the source end of

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

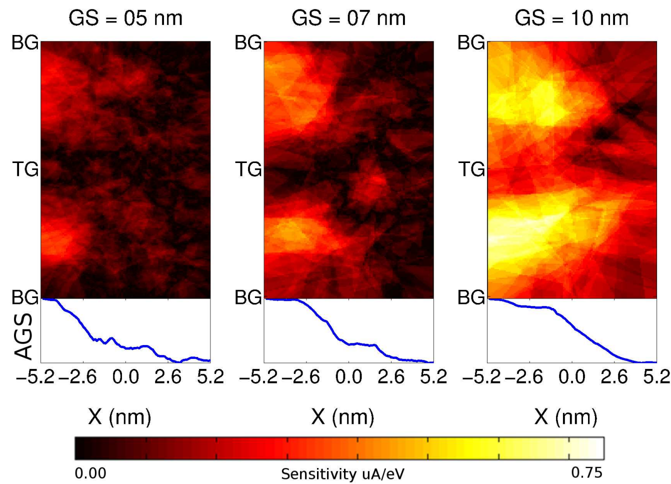


Fig. 6. 2D I_{on} FSMs for the rectangular (REC) cross-section shape $In_{0.53}Ga_{0.47}As$ FinFET at V_D=0.6 V as a function of the grain size (top) and 1D AGS along the transport direction (bottom).

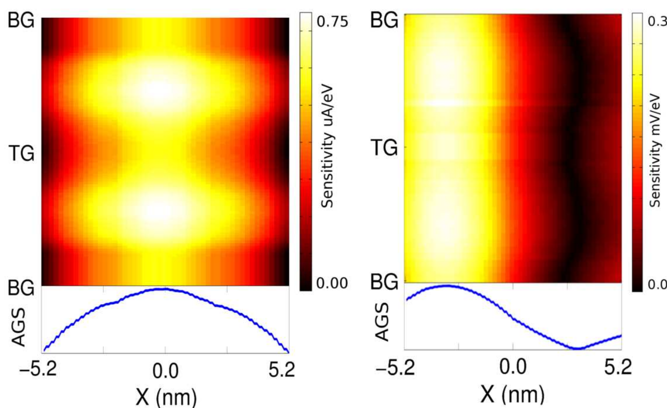


Fig. 7. 2D V_T (left) and I_{on} (right) FSMs for the REC cross-section shape $In_{0.53}Ga_{0.47}As$ FinFET for synthetic gate work-function profiles (top) and 1D AGS along the transport direction (bottom). The drain bias is 0.05 V and 0.6 V respectively.

the gate than at the drain end (see bottom plots of Fig. 6). The drain bias for the on-region analysis was set at $V_{DD} = 0.6\ V$, while it was fixed at 0.05 V in the sub-threshold region study which also explains the different behaviour observed in their respective FSM. All these effects reflect the fact that the grain size has an impact in the calculated FSM. Theoretically, the sensitivity is a characteristic of the device, but the procedure to obtain it will yield better results with bigger grains and also with more input profiles. Therefore, the smaller the grain size, the larger should be the ensemble of devices to obtain good statistical accuracy.

C. Synthetic Profiles

When using Voronoi grain distributions to extract the FSM, a concern that may arise is how independent the created map is from those very same Voronoi grains. Therefore, we have to establish whether the FSM heavily depends on the data used for its extraction. For that reason, we have created a large set of synthetic profiles that will set a fixed work-function of

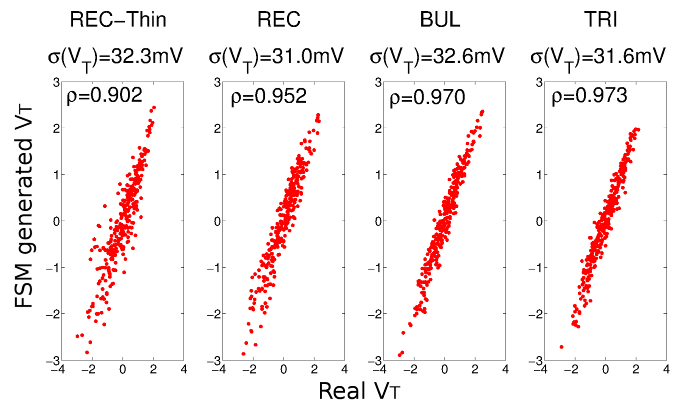


Fig. 8. Scatter plot of the predicted V_T distribution vs. the real V_T distribution using the FSM for the four analysed cross-section shapes of $In_{0.53}Ga_{0.47}As$ FinFETs. The V_T values are normalised with respect to a mean value (set at 0) and the standard deviation (set at 1). The correlation coefficient (ρ) and the standard deviation of the real distribution (σV_T) are shown for reference.

4.6 eV in the whole gate except on a vertical or a horizontal narrow strip in which the work-function is set to 4.4 eV. For instance, Fig. 3(b) shows an example of a synthetic profile that includes a horizontal strip. In order to create the FSM, firstly, the strip is placed on the gate horizontally and moved along the possible locations in the gate. Device simulations are carried out in each position and the different FoM results recorded. Then, the same process is repeated with the strip placed vertically.

Fig. 7 shows the V_T (left) and I_{ON} (right) FSM for the REC $In_{0.53}Ga_{0.47}As$ FinFET created using synthetic gate work-function profiles. These results validate the ones observed when Voronoi gate work-function profiles were used to create the fluctuation sensitivity maps as long as the grain size is large. When using the synthetic method, all the points in the gate will be uniformly inspected. For this reason, there is a perfect symmetry in the sensitivity observed from the TG to both BGs of the device as expected, whereas with Voronoi, the metal grains are randomly placed due to the nature of these metal grains. Also note that the sensitivity range for the I_{ON} FSM of the 10 nm gate $In_{0.53}Ga_{0.47}As$ FinFET is the same whether we use synthetic profiles or Voronoi profiles.

The middle of the gate ($X = 0$) work-function values are dominant contributors to the sub-threshold region variability (see the AGS in Fig. 7 left). The most significant work-function values for the MGWV in the on-region are found in the proximity of the source end of the gate, i.e., when $-5.2 < X < -1.3$ nm, the AGS$> 80\%$ (see Fig. 7 right).

The grains present on the gate will have the largest effect when aligned with the maximum of a potential barrier between the source and the drain. The maximum lies in the middle of the channel at a low drain bias but near the source at a high drain bias, as previously demonstrated by [27] for the case of a polysilicon gate MOSFET.

IV. Predictive Power of the FSM

The usefulness of the FSMs is not only limited to the spatial information that they provide. Once created, they can be also

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

employed to perform FoM variability estimations without need to simulate hundreds of different device configurations. As we have shown in the previous section, the FSMs represent the sensitivity of a device to a source of variability. Therefore, it makes sense to use them to anticipate the behaviour of a the device under different scenarios (i.e. gate configurations in the case of the MGWV). The following input parameters are necessary: i) a FSM for the device generated using either Voronoi or synthetic profiles, ii) an ensemble of P realistic gate WF profiles, and iii) the standard deviation of the FoM ($\sigma(\phi_{Real})$) obtained after the simulation of that ensemble of profiles.

When the k profile is applied, with $k = 1,2,...,P$, a FoM can be estimated via the FSM (ϕ^k_{FSM}) as follows:

$$\phi^k_{FSM} = \frac{1}{M \times N} \sum_{i,j}^{M,N} FSM_{ij} \times WF^k_{ij} \quad (4)$$

being $M \times N$ the dimension of the FSM matrix.

The real FoM simulation results (ϕ_{real}) and the ones generated via the FSM (ϕ_{FSM}) are highly correlated, as can be seen in Fig. 8, where the V_T distributions are compared for the four analysed cross-section shapes. The standard deviation of the FoM distribution estimated via the FSM ($\sigma(\phi_{FSM})$) will always be lower than the real one. This underestimation of the variability is due to the averaging process done in order to construct the FSM and it can not be eliminated. However, the mismatch (α) between the real and the FSM generated results is practically independent of the grain size and thus α can serve as a fitting parameter using the relation:

$$\sigma(\phi_{Predic}) = \alpha \times \sigma(\phi_{FSM}) \simeq \sigma(\phi_{Real}) \quad (5)$$

Initially, real simulation results are needed for an ensemble of profiles (that can be squared-shaped, Voronoi, TEM generated, etc.) in order to establish the value of α. These results will be available since it had to be previously employed to create the FSM. Once α is known, the FSM can be used to predict the variability results for the other grain sizes without need to simulate the semiconductor devices saving computational time and resources. Table I shows the V_T, I_{OFF} and I_{ON} MGWV for the 10.7 nm gate length REC Si FinFET with a TiN metal gate created via Voronoi grains. The standard deviation of the statistical distribution can been obtained by either i) simulating a large set of different devices per grain size in order to extract σ_{Real}, or ii) using the prediction provided by the FSM matrix to calculate σ_{Predic}.

On the one hand, a density-gradient quantum corrected drift-diffusion (DD) technique was used in the sub-threshold region (with simulation times in the order of a few hours) to estimate σ_{Real} for three different grain sizes, simulating 300 different device configurations per grain size [24]. However, in the on-region, a semi-classical technique like ensemble Monte Carlo (MC) had to be employed, which greatly increased the computational time. For that reason, the number of simulated device configurations per grain size was reduced to 100 [24]. The computational cost of the 1,200 sub-threshold and on-region simulations needed to extract σ_{Real} is shown in Table III.

TABLE I
THE MGWV FOR THREE DIFFERENT FOM FOR THE 10.7 NM GATE LENGTH REC SI FINFET USING EITHER SIMULATION RESULTS (σ_{Real}) OR THE FSM MATRIX GENERATED FROM VORONOI PROFILES WITH A GRAIN SIZE 10 NM (σ^{Voro}_{Predic}). THE VALUE OF THE FITTING PARAMETER (α) AND THE PERCENTAGE OF ERROR OF THE FSM-BASED ESTIMATION ARE ALSO SHOWN.

Metal	FoM	GS (nm)	α	σ_{Real}[24]	σ^{Voro}_{Predic}	Error %
TiN	V_T (mV)	10	4.2	52.40	52.40	0.0
		7		38.03	35.49	6.6
		5		26.53	24.76	6.6
	log(I_{OFF}(A))	10	4.2	0.703	0.703	0.0
		7		0.513	0.468	8.7
		5		0.366	0.327	11
	I_{ON}(μA)	10	5.3	4.460	4.460	0.0
		7		3.170	3.000	5.3
		5		2.454	1.970	19

TABLE II
THE MGWV FOR THREE DIFFERENT FOM FOR THE 10.4 NM GATE LENGTH REC $In_{0.53}Ga_{0.47}As$ FINFET USING EITHER SIMULATION RESULTS (σ_{Real}) OR THE FSM MATRIX GENERATED FROM SYNTHETIC PROFILES (σ^{Synt}_{Predic}). THE VALUE OF THE FITTING PARAMETER (α) AND THE PERCENTAGE OF ERROR OF THE FSM-BASED ESTIMATION ARE ALSO SHOWN.

Metal	FoM	GS (nm)	α	σ_{Real}[24]	σ^{Synt}_{Predic}	Error %
TiN	V_T (mV)	10	5.5	41.22	41.22	0.0
		7		30.06	28.50	5.2
		5		21.47	19.36	9.8
	log(I_{OFF}(A))	10	5.5	0.531	0.531	0.0
		7		0.389	0.372	4.3
		5		0.280	0.252	9.8
	I_{ON}(μA)	10	6.2	10.20	10.20	0.0
		7		7.074	7.461	5.5
		5		5.647	5.294	6.2
WN	V_T (mV)	10	10.5	120.3	120.3	0.0
		7		87.97	83.91	4.6
		5		68.83	60.91	11

On the other hand, the FSM generated from Voronoi profiles can be used to calculate σ^{Voro}_{Predic} (see results in Table I). For that, we are just simulating the ensemble of profiles for a particular grain size (in our case 10 nm), and the variability results for the other possible grain sizes are just computed. Therefore, the number of required simulations decreases to 400; 300 of them are needed to extract a FSM and α for the sub-threshold region

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

TABLE III

COMPARISON OF THE TOTAL COMPUTATIONAL COST OF PERFORMING THE SUB-THRESHOLD (VIA *DD* SIMULATIONS [22]) AND ON-REGION (VIA *MC* SIMULATIONS [25]) FOR THE TIN MGW VARIABILITY STUDY PRESENTED IN TABLES I AND II. THE TOTAL TIME OF THE REAL SIMULATIONS (σ_{Real}) IS COMPARED TO THAT OF THE FSM PREDICTIONS GENERATED VIA EITHER VORONOI PROFILES (σ^{Voro}_{Predic}) OR SYNTHETIC ONES (σ^{Synt}_{Predic}). *FSM time* INDICATES THE TIME SPENT IN THE GENERATION OF THE FSM MAP AND IN THE CALCULATION OF THE PREDICTION. THE RESULTS ARE OBTAINED ON INTEL i5 − 2500 PROCESSORS AT 3.3 GHZ.

	Sim. method	No. sim.	No. GS	Sim. time (1 core)	FSM time	Total time
σ_{Real}	DD	300	3	6 hr	0	5400 hr
	MC	100	3	24 hr	0	7200 hr
σ^{Voro}_{Predic}	DD	300	1	6 hr	2 min	1800 hr
	MC	100	1	24 hr	2 min	2400 hr
σ^{Synt}_{Predic}	DD	460	1	6 hr	2 min	2760 hr
	MC	260	1	24 hr	2 min	6240 hr

and the other 100 to extract an on-region FSM and α. Note that the same FSM cannot be used for both sub-threshold and on-region FoMs because of their different sensitivity regions (as shown in Fig. 7). When using this method to analyse the MGW variability, the computational cost is reduced by a factor of 3 as seen in Table III. Table I presents the percentage of error in the standard deviation when the FSM is used to calculate the MGWV which is lower than 12% in most of the analysed cases. In order to calculate the error, we have used the variability results for a 10 nm grain size as a fitting parameter (which explains the 0% error shown in the Table) because, the larger the grain size, the less simulations are needed to obtain statistical significance (see, for instance, Fig. 6). Note that, for the smaller grain size of 5 nm, the error in the on-current prediction increases to 19%, because only 100 samples were available to create the FSM.

Furthermore, synthetic gate profiles can be utilised to create the FSM, and they will also have a predictive power. For instance, the V_T, I_{OFF} and I_{ON} MGWV are presented in Table II for the 10.4 nm gate length REC $In_{0.53}Ga_{0.47}As$ FinFET with a TiN metal gate. The V_T variability as a function of the grain size for a WN metal gate has also been included. When using synthetic profiles to create the FSM, there is an extra computational cost (see Table III). In our particular case, 160 extra simulations were needed to sweep the gate of the device and create the synthetic fluctuation sensitivity map but this very same map can be then used for any kind of realistic gate work-function profiles (square, Voronoi, TEM generated, etc.) with different grain sizes and even with different metal gates (see Table II for TiN and WN). The percentage of error in the standard deviation, when the synthetic FSM is used to calculate the MGWV, is lower than 12% in all the analysed cases including the on-current when the grain size is 5 nm, because the synthetic FSM does not have the random nature inherent to the Voronoi generated FSM.

V. CONCLUSION

A novel technique based on the creation of a Fluctuation Sensitivity Map (FSM) has been presented for the investigation of intrinsic sources of variability in semiconductor devices. The FSM yields spatial information that could not be obtained via the existing exclusively statistical techniques. Specifically, the FSM provides information on sensitivity of different regions of a semiconductor device to a certain source of variability. This technique, which can be applied to different simulation models, can assist in the design of variability-resistant device architectures significantly shortening time for their research and development.

The FSM technique has been applied to study the Metal Grain Work-function Variability (MGWV) affecting state-of-the-art FinFETs to demonstrate its advantages. We have demonstrated that this technique helps to decrease the computational cost of statistical study because, once the original FSM is created, the map can be used to predict the MGWV for different FoMs, metal gate materials or their grain sizes, with estimation errors generally smaller than 12%.

REFERENCES

[1] N. Agrawal, Y. Kimura, R. Arghavani and S. Datta, "Impact of transistor architecture (bulk planar, trigate on bulk, ultrathin-body planar SOI) and material (silicon or III-V semiconductor) on variation for logic and SRAM applications", *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3298-3304, 2013.

[2] S. H. Rasouli, K. Endo, and K. Banerjee, "Work-Function variation induced fluctuation in bias-temperature-instability characteristics of emerging metal-gate devices and implications for digital design", in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 714-720, 2010.

[3] S. Agarwal, R. K. Pandey, J. B. Johnson, A. Dixit, M. Bajaj, S. S. Furkay, P. J. Oldiges, K. V. R. M. Murali, "Ab initio study of metal grain orientation-dependent work function and its impact on FinFET variability", *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2728-2733, 2013.

[4] G. Leung and C. O. Chui, "Variability of inversion-mode and junctionless FinFETs due to line edge roughness", *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1489-1491, 2011.

[5] D. Reid, C. Millar, S. Roy and A. Asenov, "Understanding LER-Induced MOSFET Vt variability", *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2801-2807, 2010.

[6] N. Seoane, G. Indalecio, E. Comesana, M. Aldegunde, A. J. Garcia-Loureiro, and K. Kalna, "Random dopant, line-edge roughness, and gate workfunction variability in a nano InGaAs FinFET", *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 466-472, 2014.

[7] A. Martinez, M. Aldegunde, N. Seoane, A.R. Brown and A. Asenov, "Quantum transport study on the impact of channel length and cross sections on variability induced by random discrete dopants in narrow gate-all-around silicon nanowire transistors", *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2209-2217, 2011.

[8] X. Wang, A. R. Brown, B. Cheng and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs", *IEDM Tech. Dig.*, pp. 103-106, 2011.

[9] N. Seoane, G. Indalecio, E. Comesaña, A. J. García-Loureiro, M. Aldegunde and K. Kalna, "Three-dimensional simulations of random dopant and metal-gate workfunction variability in an $In_{0.53}Ga_{0.47}As$ GAA MOSFET", *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 205-207, 2013.

[10] M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "3D finite element Monte Carlo simulations of multigate nanoscale Transistors", *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561-1567, 2013.

[11] N. Seoane, M. Aldegunde, K. Kalna, and A. J. Garcia-Loureiro, "MC/DD study of metal grain induced current variability in a nanoscale InGaAs FinFET", *in Int. Conference on Simulation of Semiconductor Processes and Devices, SISPAD*, pp. 253-256, 2014.

© 2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. A definitive version was subsequently published in IEEE Transactions on Electron Devices, Vol. 46, No. 4, 2017, DOI: 10.1109/TED.2017.2670060.

[12] A. Wettstein, O. Penzin, E. Lyumkis, and W. Fichtner, "Random dopant fluctuation modelling with the impedance field method", *in Int. Conference on Simulation of Semiconductor Processes and Devices, SISPAD*, Sept. 2003.

[13] D. Reid, C. Millar, G. Roy, S. Roy and A. Asenov, "Analysis of Threshold Voltage Distribution Due to Random Dopants: A 100,000-Sample 3-D Simulation Study", *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2255 - 2263, 2009.

[14] V. S. Basker et al., "A 0.063 m^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch", *in Symposium on VLSI Technology. IEEE*, pp. 19-20, 2010.

[15] G. Patton, "Evolution and expansion of SOI in VLSI technologies: Planar to 3D", *in IEEE International SOI Conference (SOI). IEEE*, pp. 1-40, 2012.

[16] D. Nagy, M. A. Elmessary, M. Aldegunde, R. Valin, A. Martinez, J. Lindberg, W. G. Dettmer, D. Perić, A. J. García-Loureiro, and K. Kalna, "3D finite element Monte Carlo simulations of scaled Si SOI FinFET with different cross-sections", *IEEE Trans. Nanotechnol.*, vol. 14, no. 1, pp. 93-100, Jan. 2015.

[17] International Technology Roadmap for Semiconductors (ITRS), 2013.

[18] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors–Part I: modeling, analysis, and experimental validation", *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504-2514, 2010.

[19] G. Indalecio, M. Aldegunde, N. Seoane, K. Kalna, and A. J. Garcia-Loureiro, "Statistical study of the influence of LER and MGG in SOI MOSFET", *Semicond. Sci. Technol.*, vol. 29, pp. 045005 (7pp), 2014.

[20] S.-H. Chou, M.-L. Fan, P. Su, "Investigation and Comparison of Work Function Variation for FinFET and UTB SOI Devices Using a Voronoi Approach", *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1485-1489, 2013.

[21] G. Indalecio, A. J. Garcia-Loureiro, N. Seoane, and K. Kalna, "Study of Metal-Gate Work-Function Variation Using Voronoi Cells: Comparison of Rayleigh and Gamma Distributions", *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2625-2628, 2016.

[22] A. J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez, and K. Kalna, "Implementation of the density gradient quantum corrections for 3-d simulations of multigate nanoscaled transistors", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 6, pp. 841-851, 2011.

[23] ATLAS Users Manual, Silvaco Inc., pp. 13-1-24, 2012.

[24] N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmessary, A. J. Garcia-Loureiro, and K. Kalna, "Comparison of Fin-Edge Roughness and Metal Grain Work Function Variability in InGaAs and Si FinFETs", *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209-1216, 2016.

[25] N. Seoane, M. Aldegunde, D. Nagy, M. A. Elmessary, G. Indalecio, A. J. Garcia-Loureiro and K. Kalna, "Simulation study of scaled $In_{0.53}Ga_{0.47}As$ and Si FinFETs for sub-16 nm technology nodes", *Semicond. Sci. Technol.*, vol.31, pp. 075005 (7pp), 2016.

[26] N. Seoane, G. Indalecio, K. Kalna, and A. J. Garcia-Loureiro, "Impact of cross-section of 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ on metal grain variability", *in Int. Conference on Simulation of Semiconductor Processes and Devices, SISPAD*, Sept. 2016.

[27] M. Aldegunde, A. J. Garcia-Loureiro, K. Kalna and A. Asenov, "Study of fluctuations in advanced MOSFETs using a 3D finite element parallel simulator", *J. Comput. Electron*, vol. 5, pp. 311-314, 2006.

View publication stats